

A circular black ink stamp from the Canadian Intellectual Property Office (CIPO). The text "CIPO" is at the top, "JUN 24 2003" is in the center, and "PATENT & TRADEMARK OFFICE" is at the bottom. The number "3025" is on the right side.

6696898

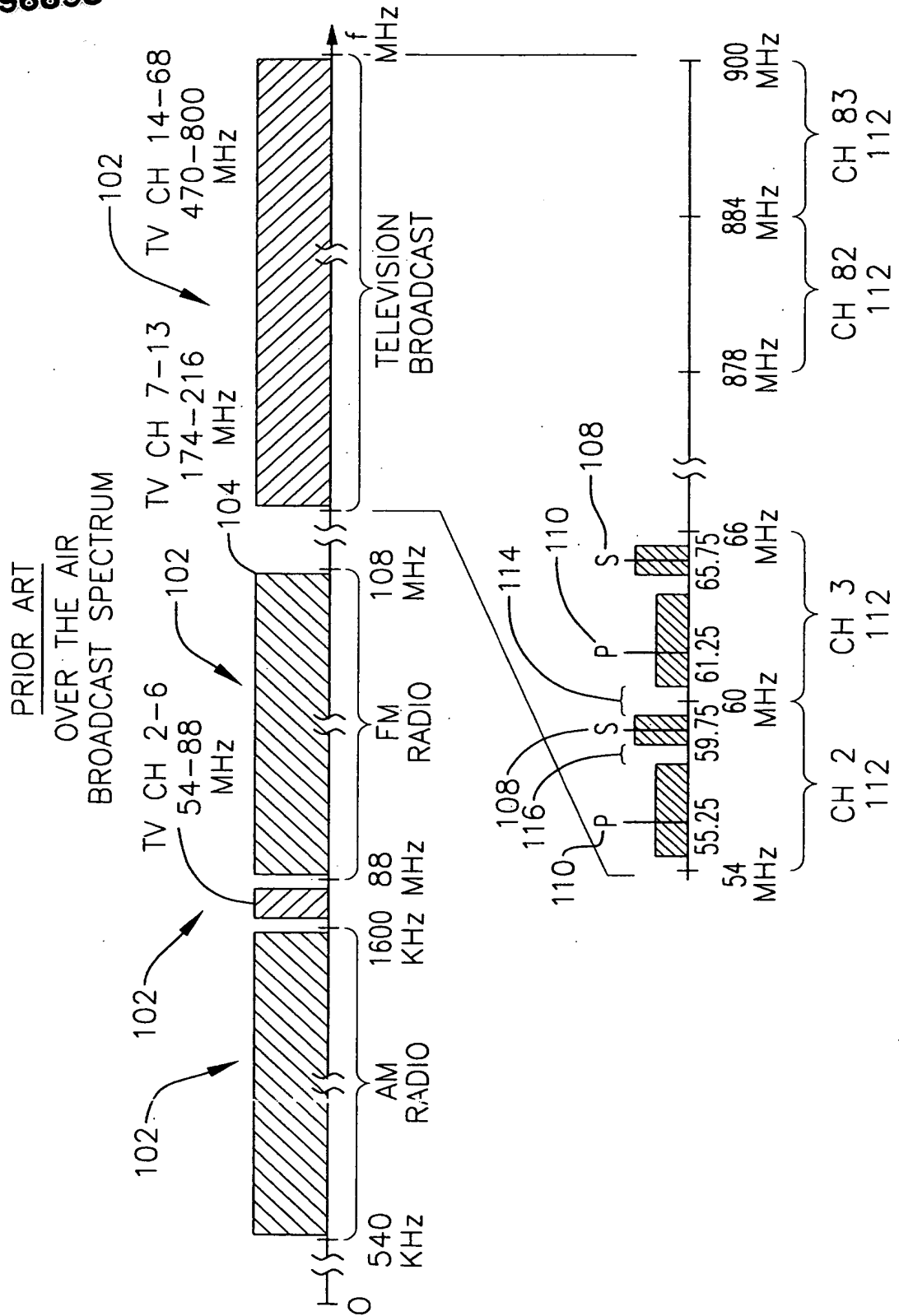




FIG. 2

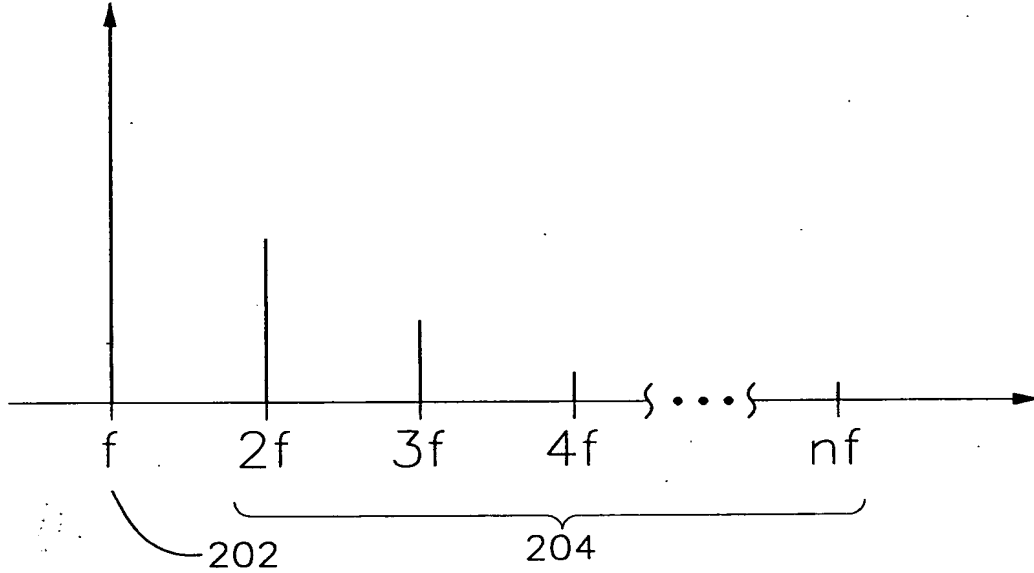


FIG. 3

PRIOR ART

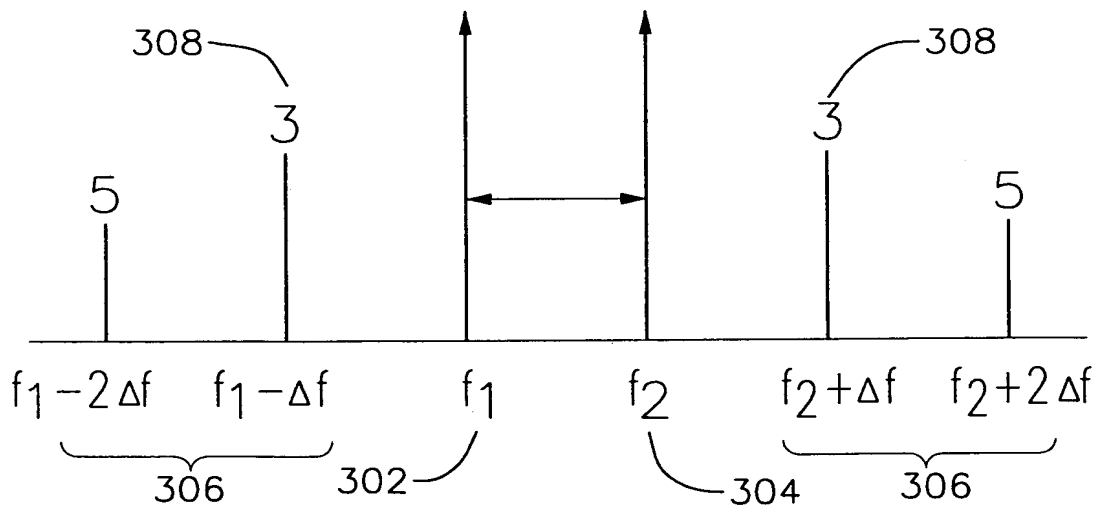




FIG. 4
 PRIOR ART

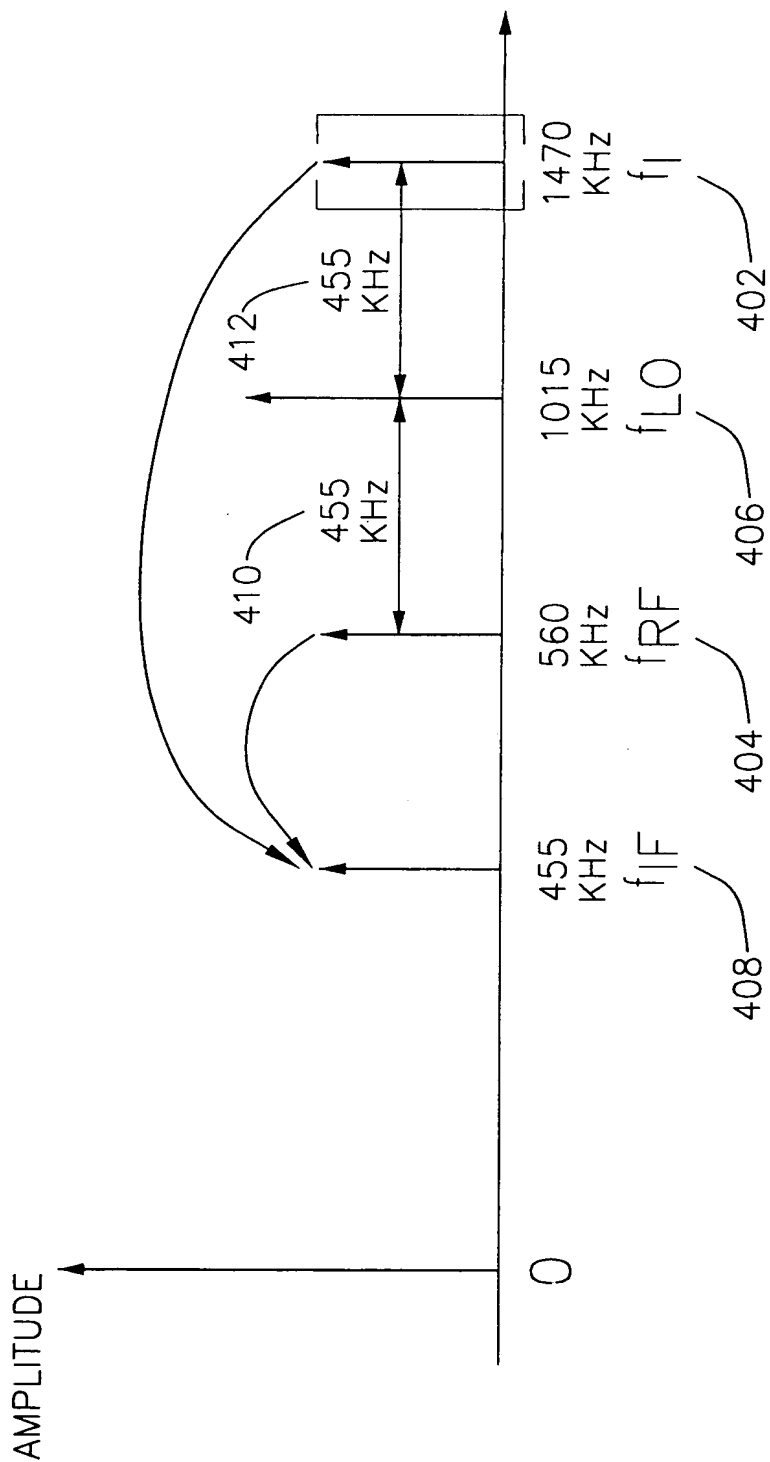




FIG. 5
 DUAL CONVERSION RECEIVER

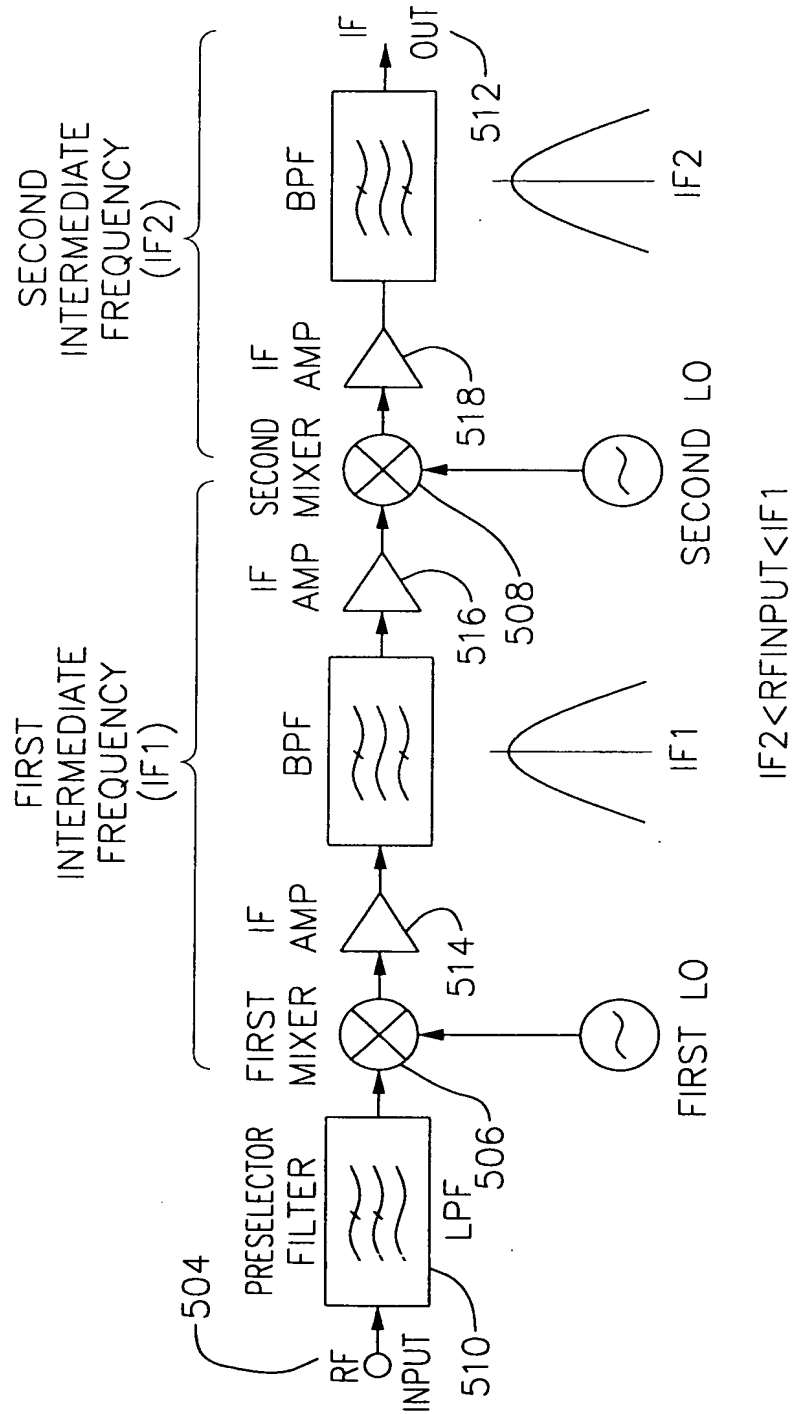




FIG. 6

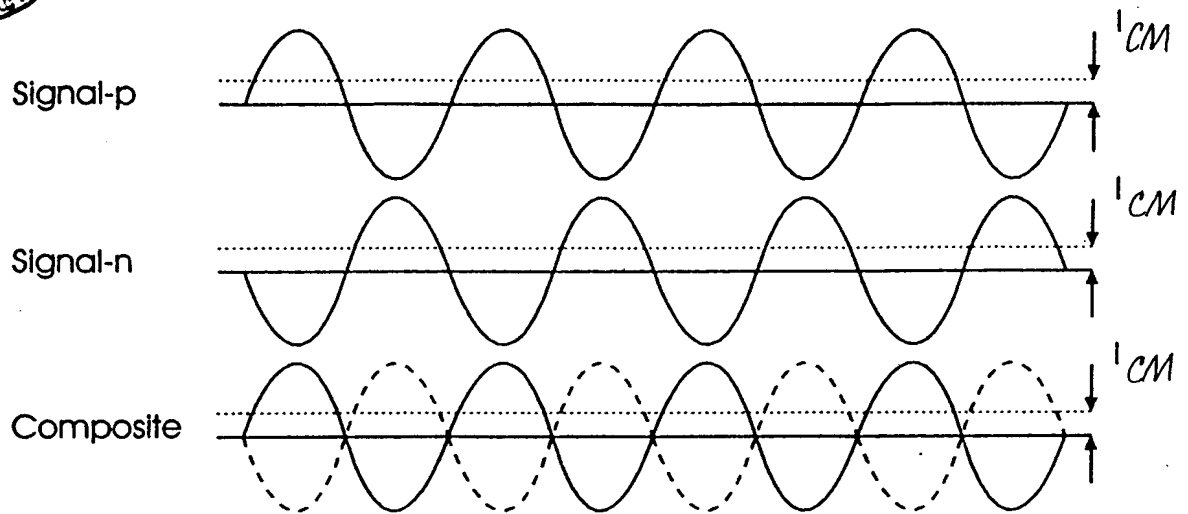


FIG. 7

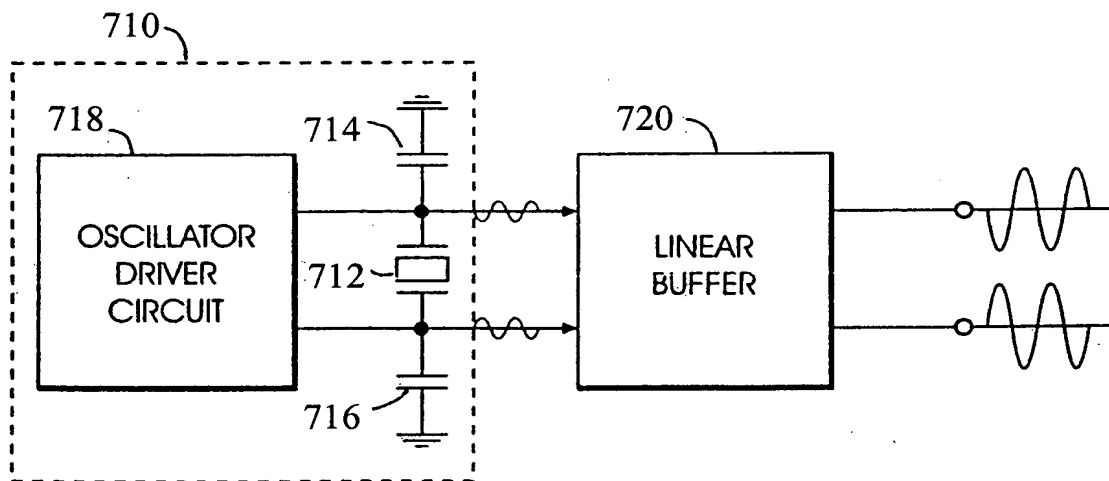




FIG. 8

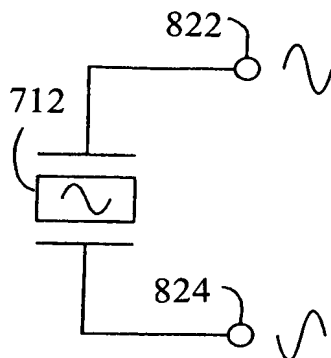


FIG. 9

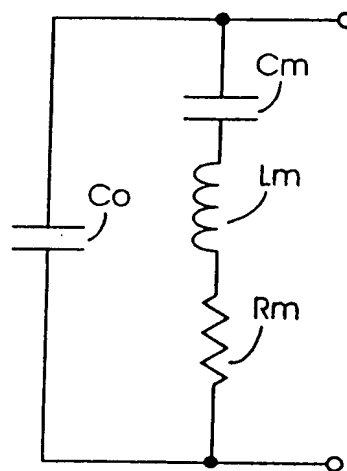


FIG. 10

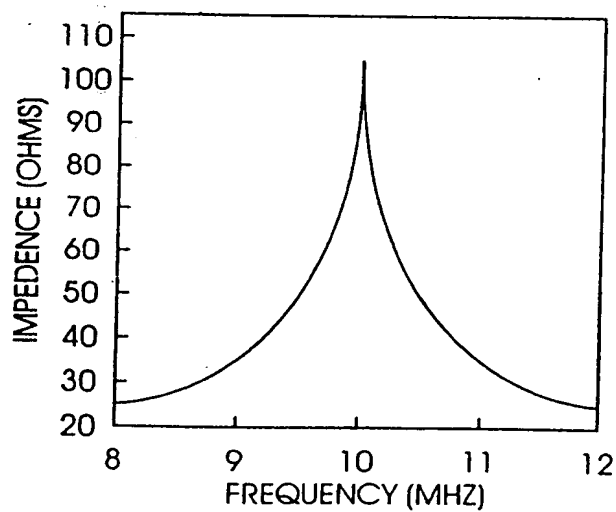
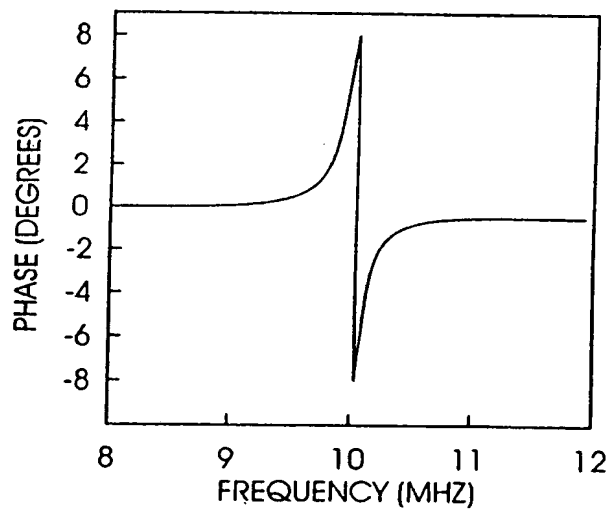


FIG. 11



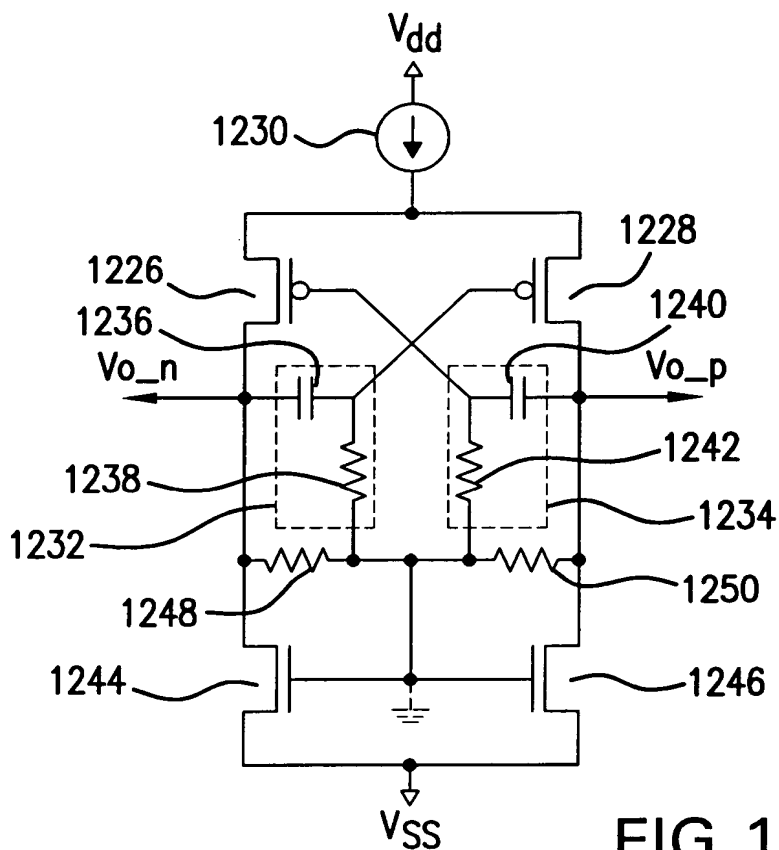


FIG. 12

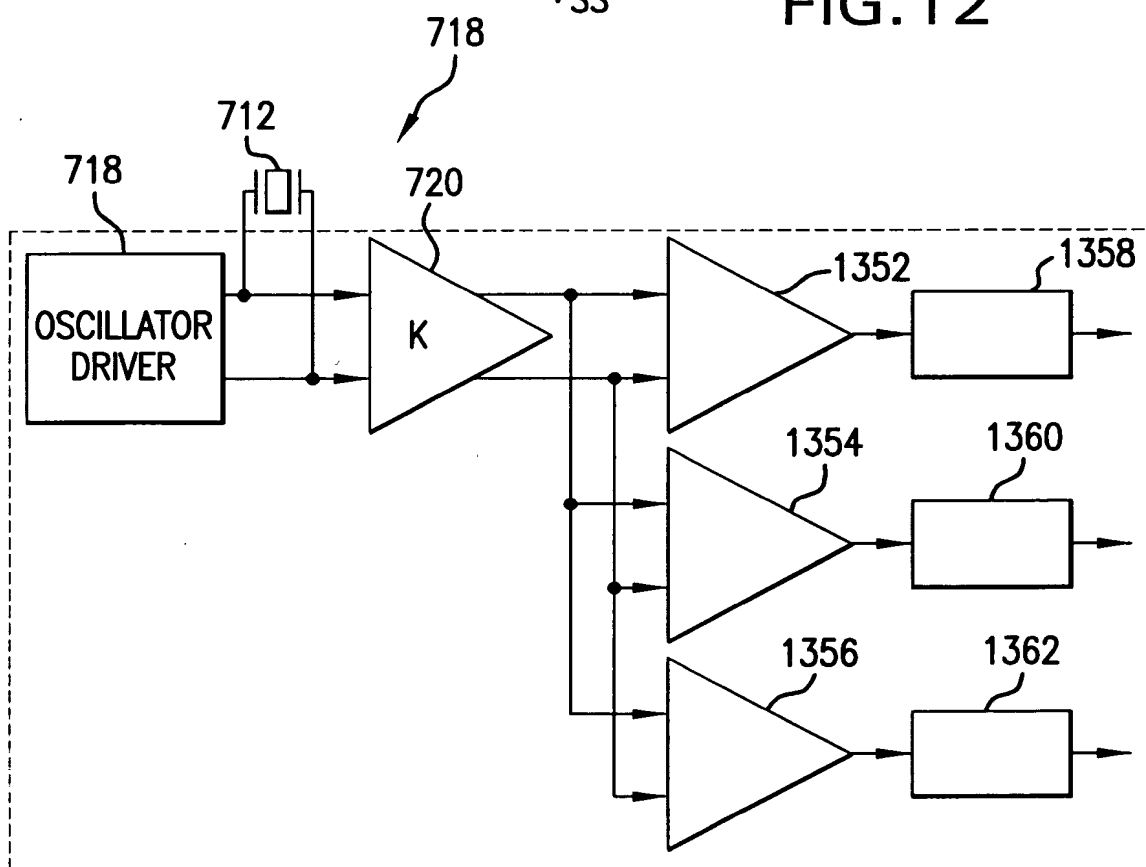
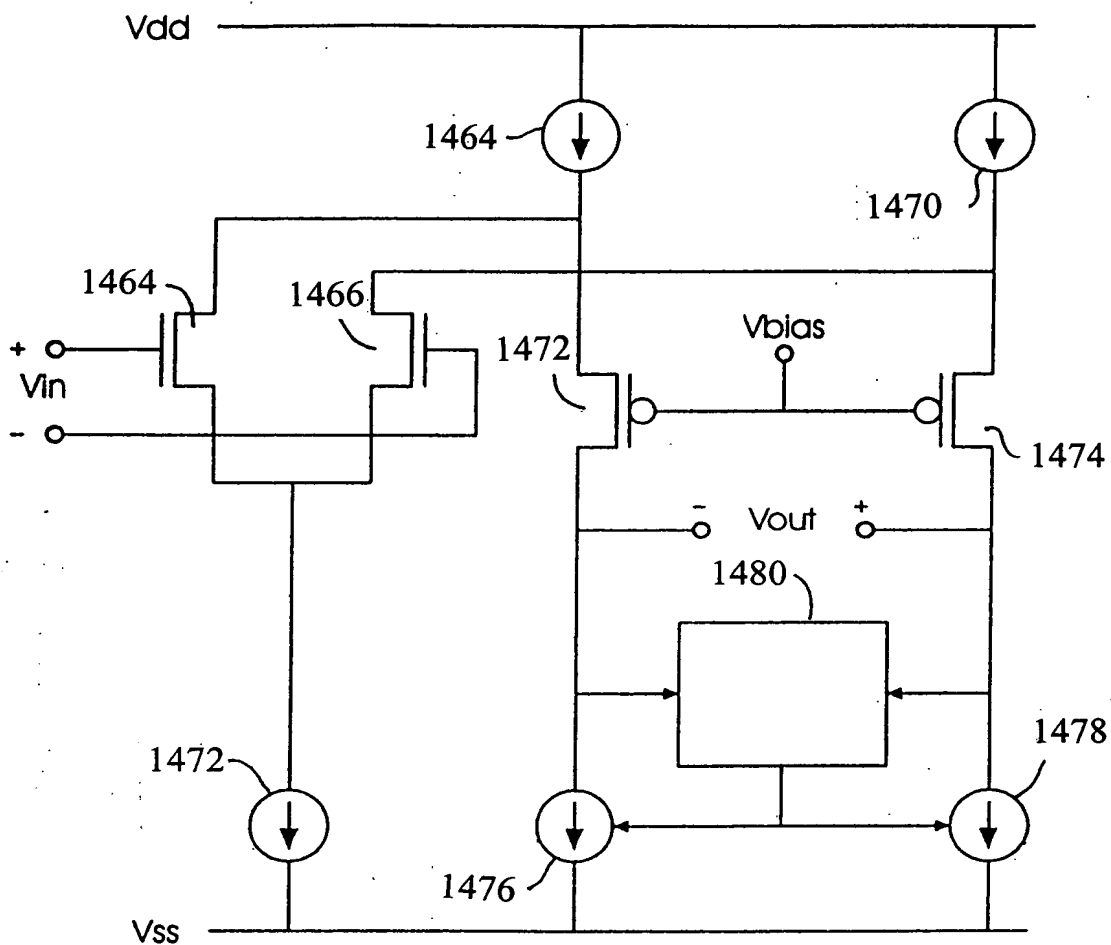


FIG. 13



FIG. 14



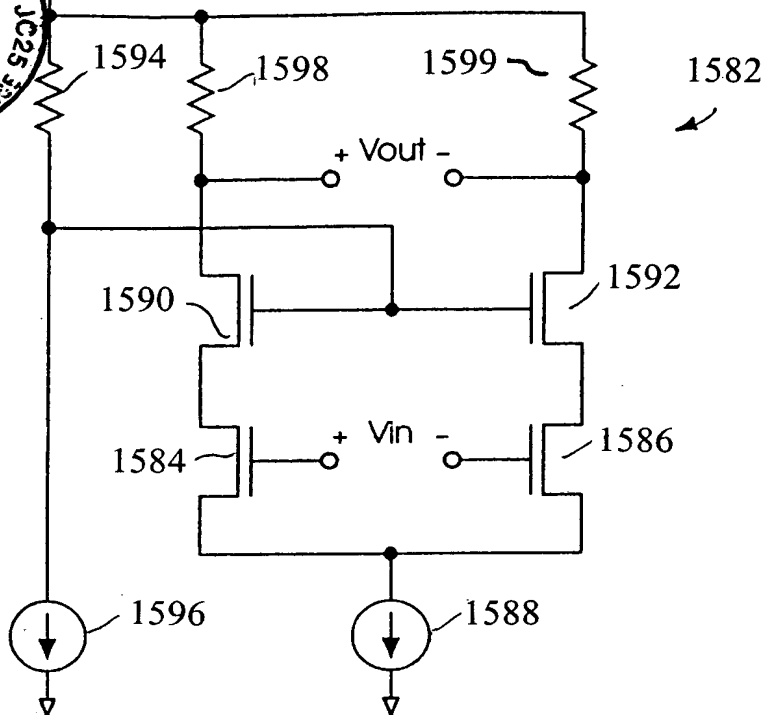
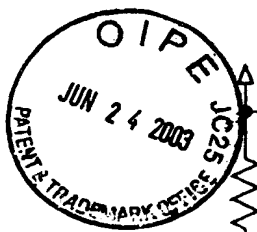


FIG. 15

FIG. 16

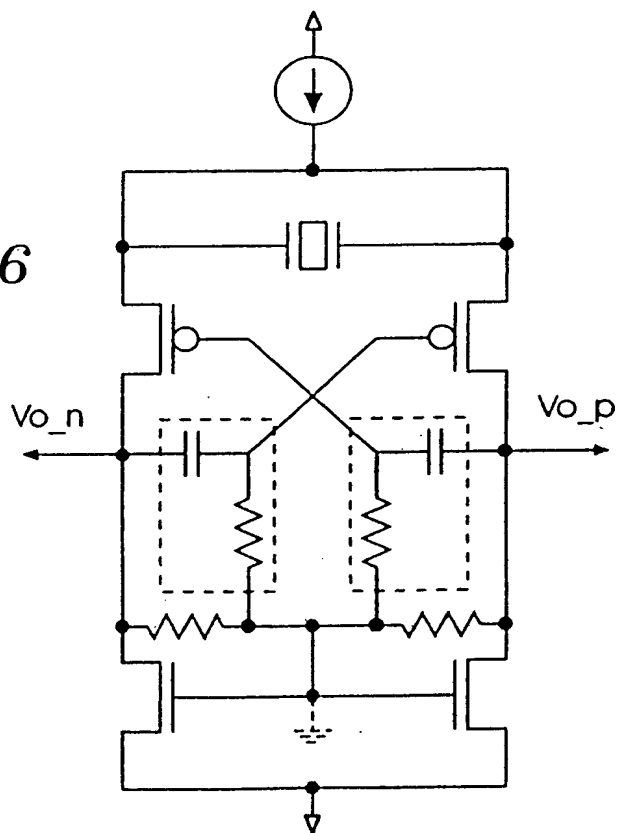




FIG. 17

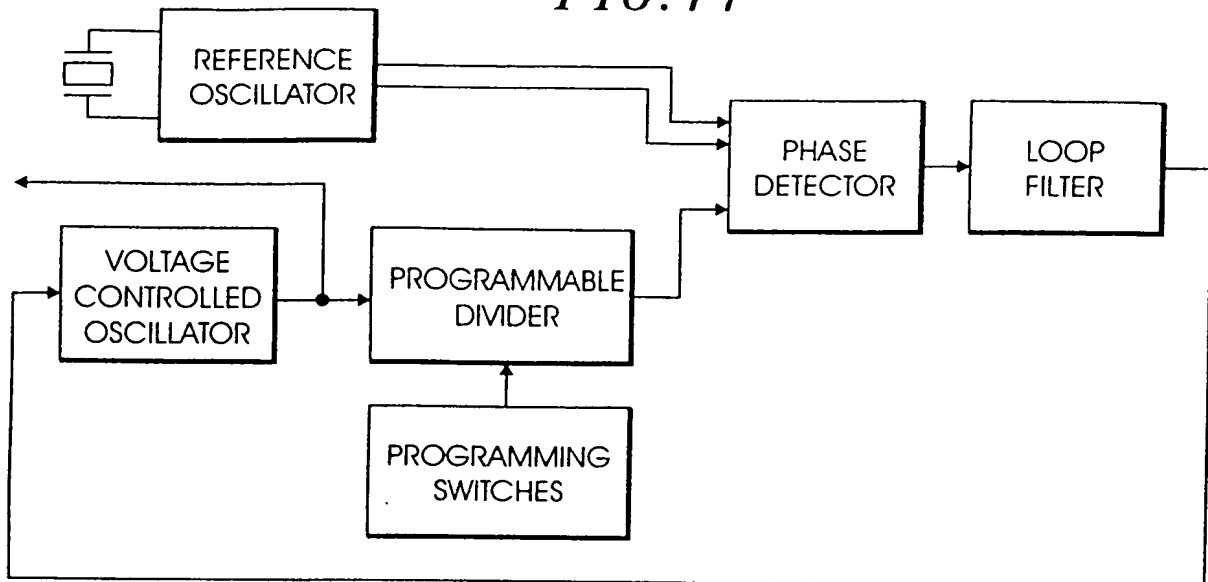


FIG. 18

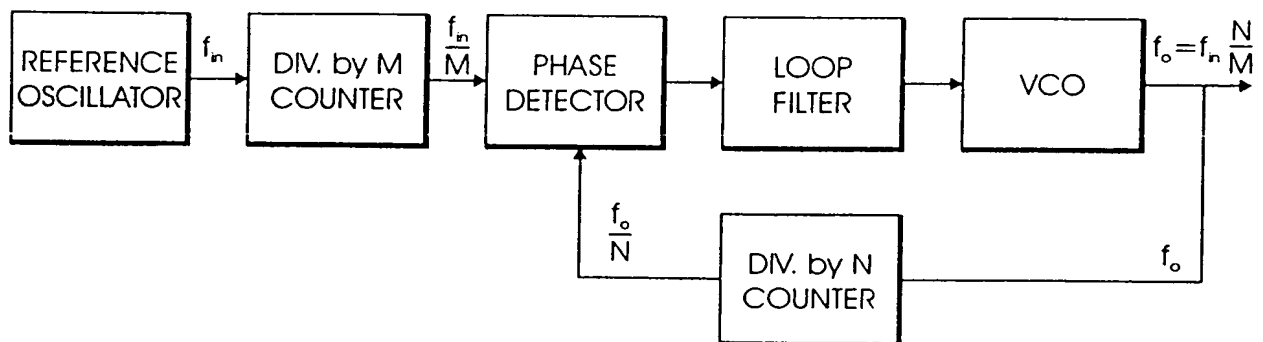


FIG. 19

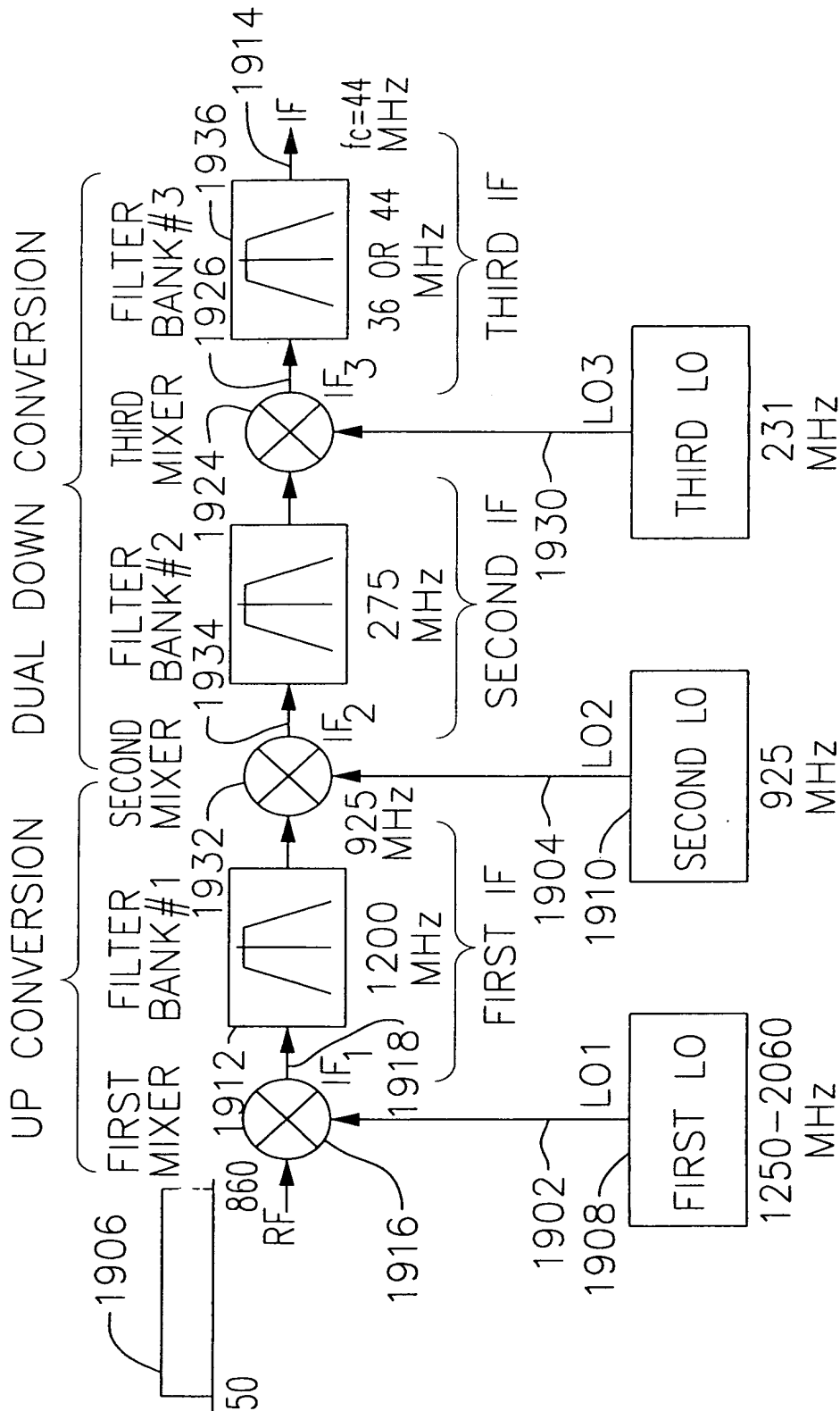




FIG. 20

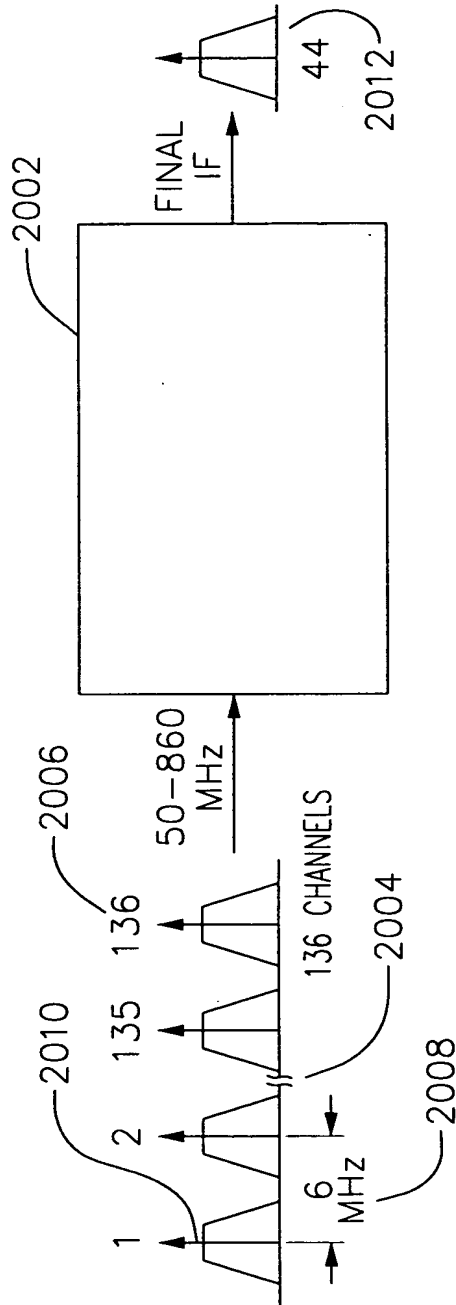




FIG. 21

PPL XtoI REFERENCE=10MHz
 LO-1, 10MHz FREQUENCY STEPS
 LO-2, 100kHz FREQUENCY STEPS

44MHz IF

NOTE
 • LO-2 REF=100KHz,
 SO DIVIDE RANGE=9216 TO 9280

TABLE OF FREQUENCIES BASED ON
 COARSE/FINE PLL SOLUTION:

Frq (MHz)	50	56	62	68	74	80	86	92	98	104	110	116	122	128	"	854	860
LO-1(MHz)	1250	1260	1260	1270	1270	1280	1290	1290	1300	1300	1310	1320	1320	1330	"	2050	2060
IF-1 (MHz)	1200	1204	1198	1202	1196	1200	1204	1198	1202	1196	1200	1204	1198	1202	"	1196	1200
LO-2(MHz)	924.8	928.0	923.2	926.4	921.6	924.8	928.0	923.2	926.4	921.6	924.8	928.0	923.2	926.4	"	921.6	924.8
IF-2(MHz)	275.2	276.0	274.8	275.6	274.4	275.2	276.0	274.8	275.6	274.4	275.2	276.0	274.8	275.6	"	274.4	275.2
LO-3(MHz)	231.2	232	230.8	232	230	231	232	231	232	230	231	232	231	232	"	230	231
IF-3(MHz)	44.0	44.0	44.0	44.0	44.0	44.0	44.0	44.0	44.0	44.0	44.0	44.0	44.0	44.0	"	44.0	44.0

2102



FIG. 22

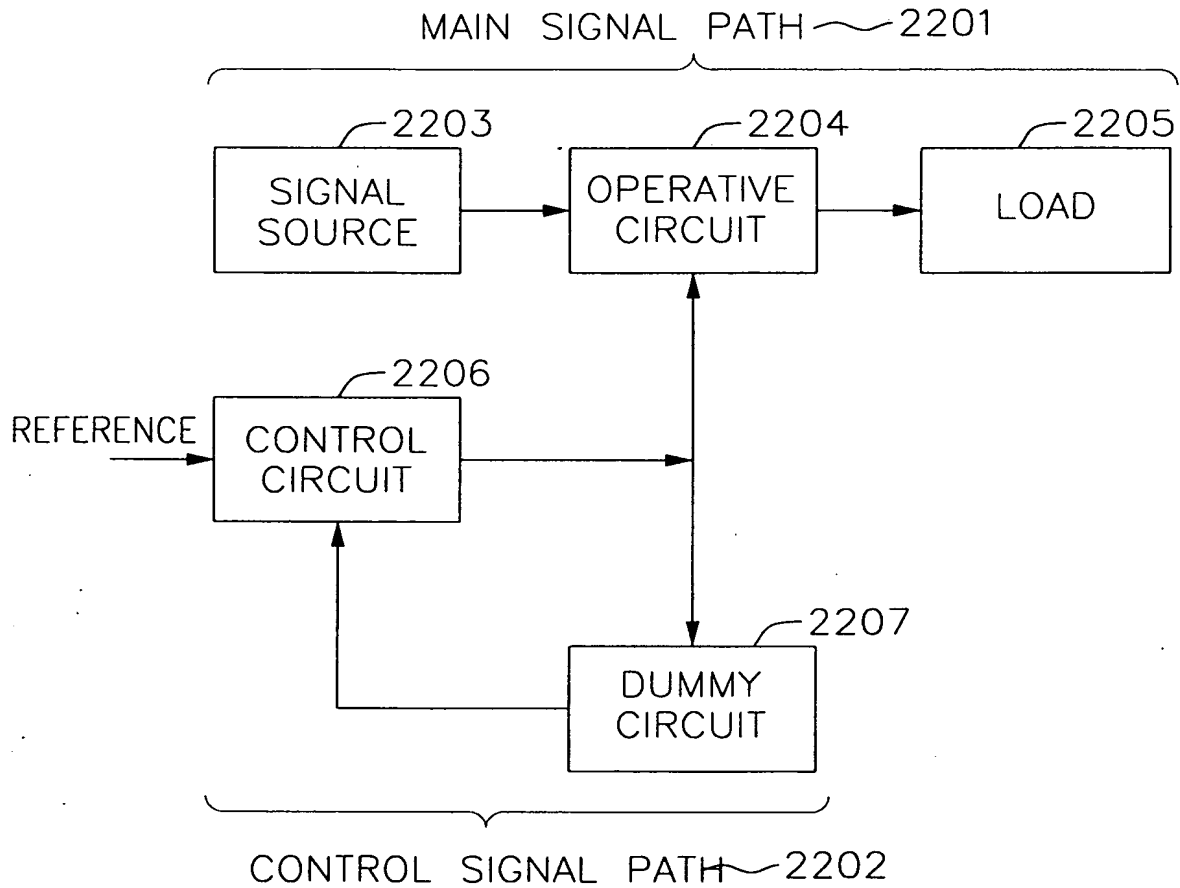
PPL Xtal REFERENCE=10MHz
 LO-1, 10MHz FREQUENCY STEPS
 LO-2, 100kHz FREQUENCY STEPS

36MHz IF

NOTE
 • LO-2 REF=100KHz,
 SO DIVIDE RANGE=9280 TO 9340

TABLE OF FREQUENCIES BASED ON
 COARSE/FINE PLL SOLUTION:

Frf (MHz)	50	58	66	74	82	90	98	106	114	122	130	138	146	154	"	852	860
LO-1(MHz)	1250	1260	1270	1270	1280	1290	1300	1310	1310	1320	1330	1340	1350	1350	"	2050	2060
IF-1 (MHz)	1200	1202	1204	1196	1198	1200	1202	1204	1196	1198	1200	1202	1204	1196	"	1198	1200
LO-2(MHz)	931.2	932.8	934.4	928.0	930	931	933	934	928.0	930	931	933	934	928.0	"	929.60	931.2
IF-2(MHz)	268.8	269.2	269.6	268.0	268.4	268.8	269.2	269.6	268.0	268.4	268.8	269.2	269.6	268.0	"	268.4	268.8
LO-3(MHz)	232.8	233.2	233.6	232	232	233	233	234	232	232	233	233	234	232.0	"	232.4	232.8
IF-3(MHz)	36.0	36.0	36.0	36.0	36.0	36.0	36.0	36.0	36.0	36.0	36.0	36.0	36.0	36.0	"	36.0	36.0

*FIG. 23*

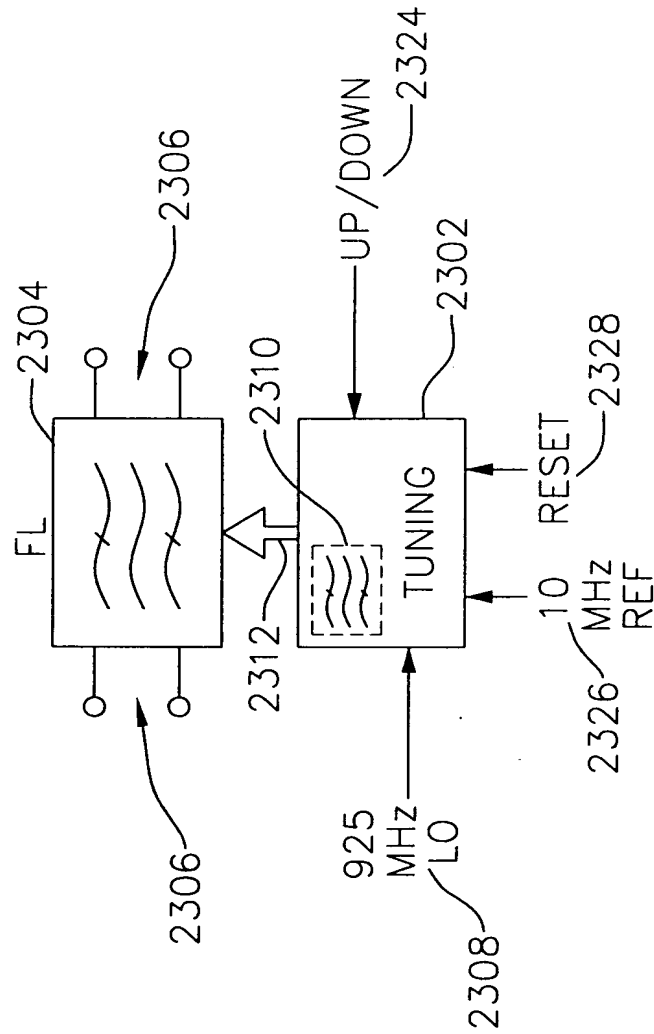
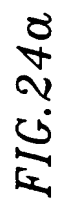




FIG. 24b

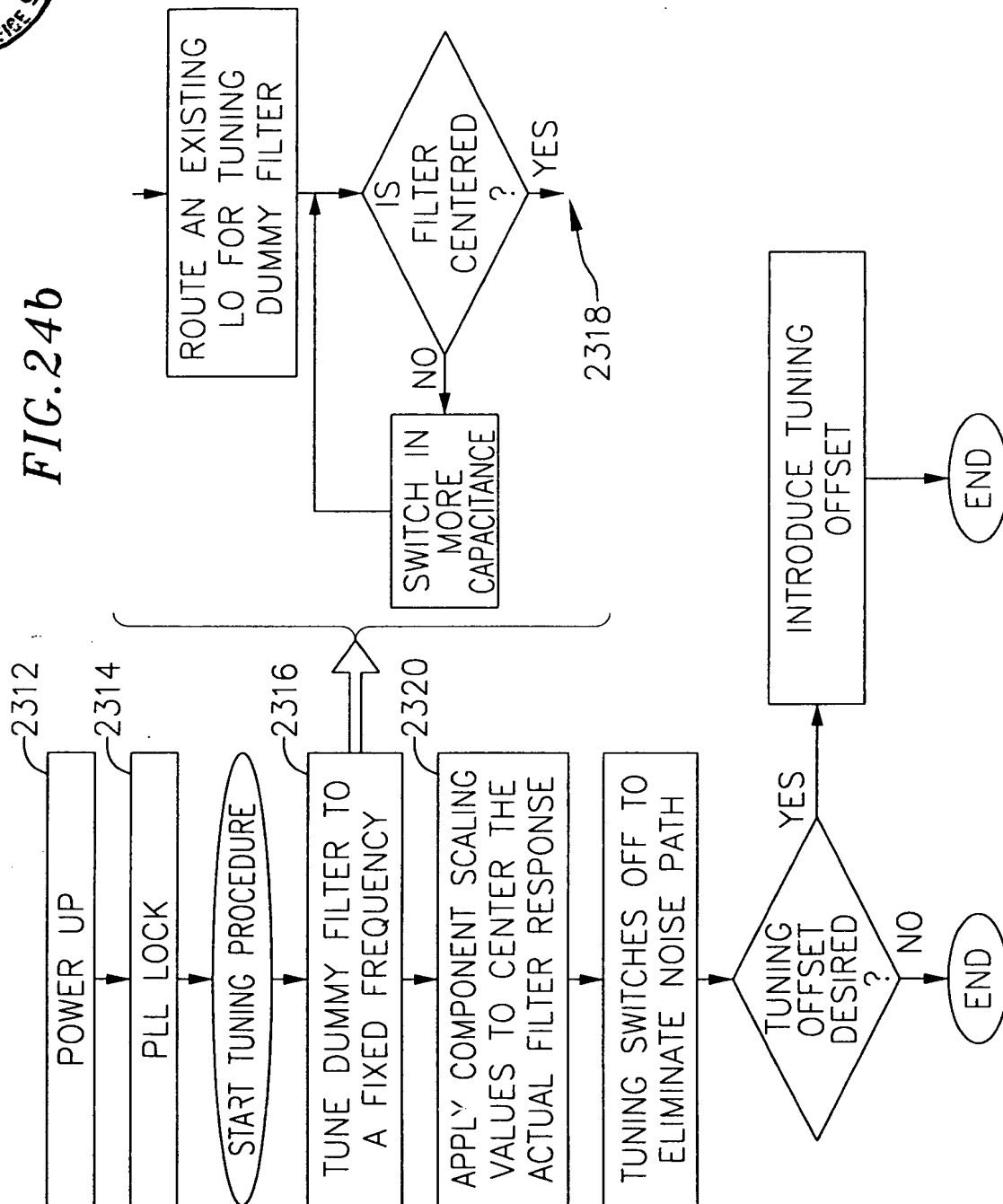




FIG. 24c

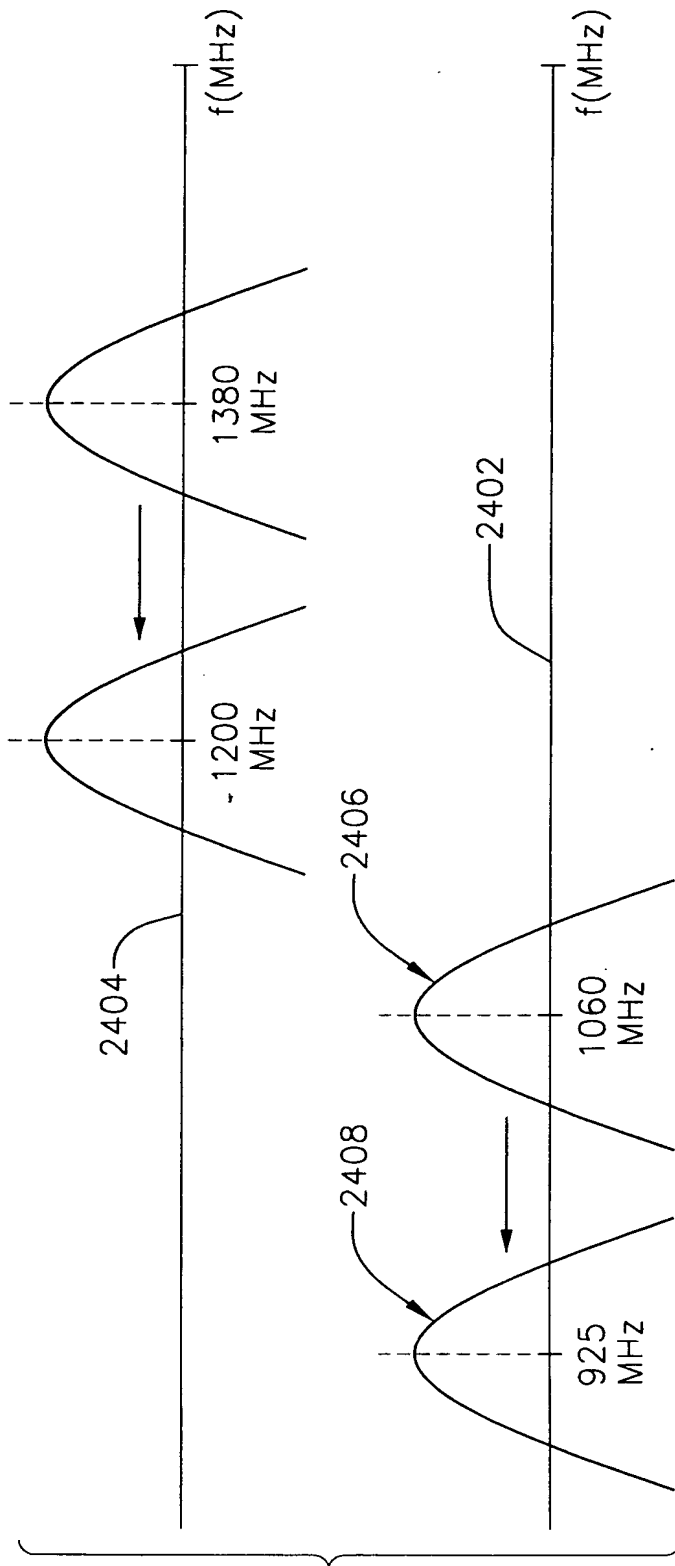




FIG. 25

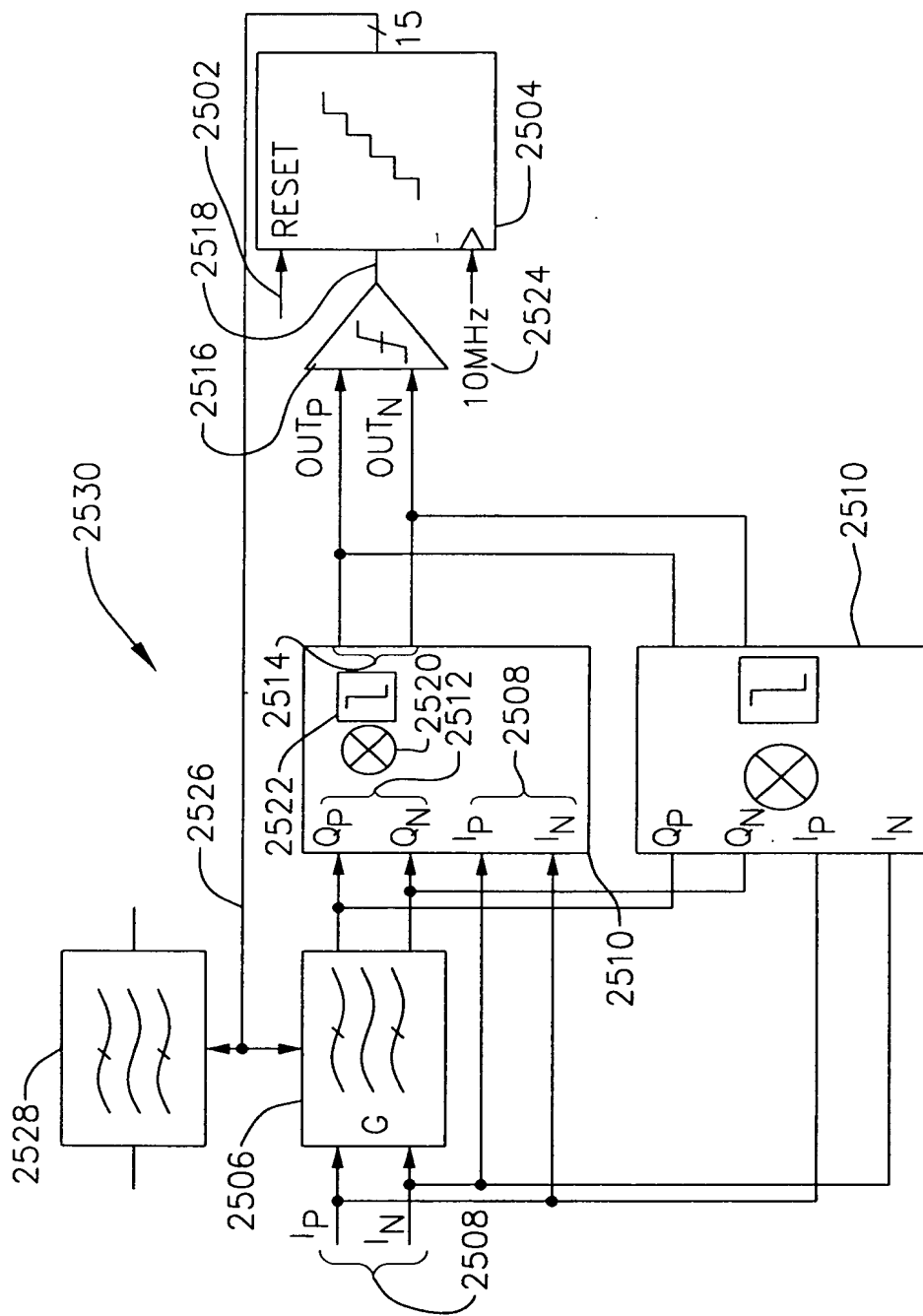




FIG. 26

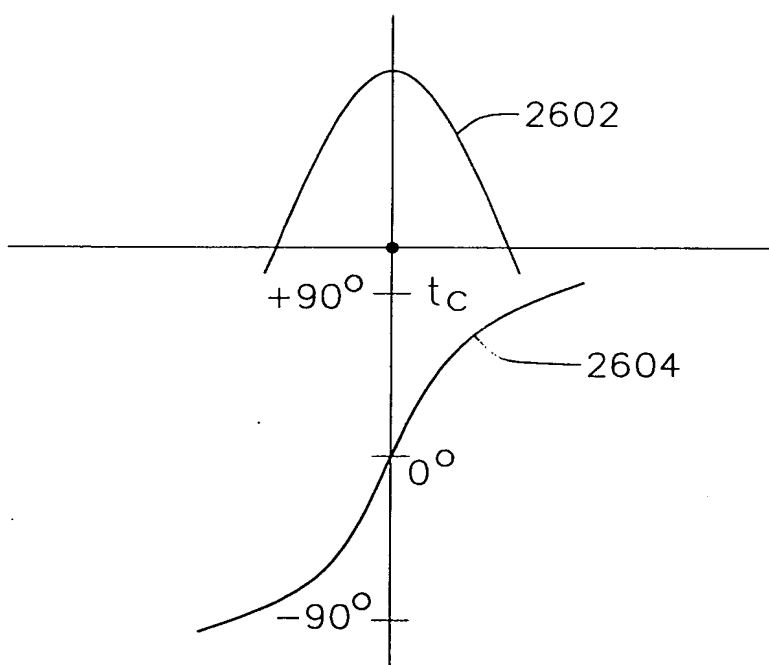
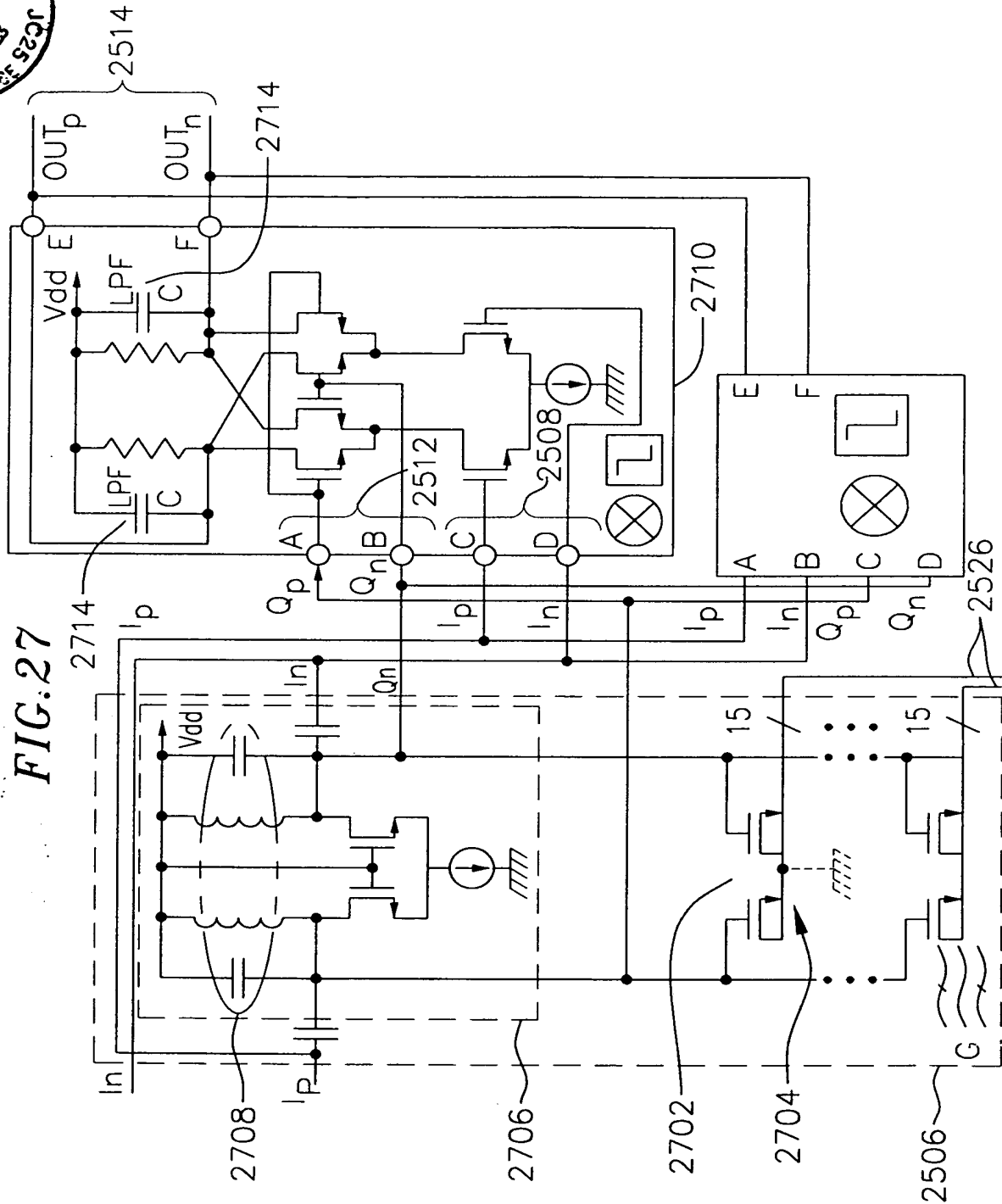


FIG. 27



Appl. No. 09/438,689; Filed: November 12, 1999
Dkt. No. 1875.095000C; Group Art Unit: 2817
Inventors: Ward *et al.*; Tel: 202/371-2600
Title: Differential Crystal Oscillator



FIG. 28

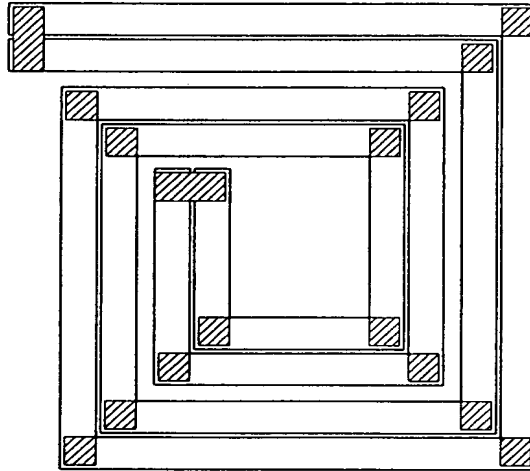




FIG. 29

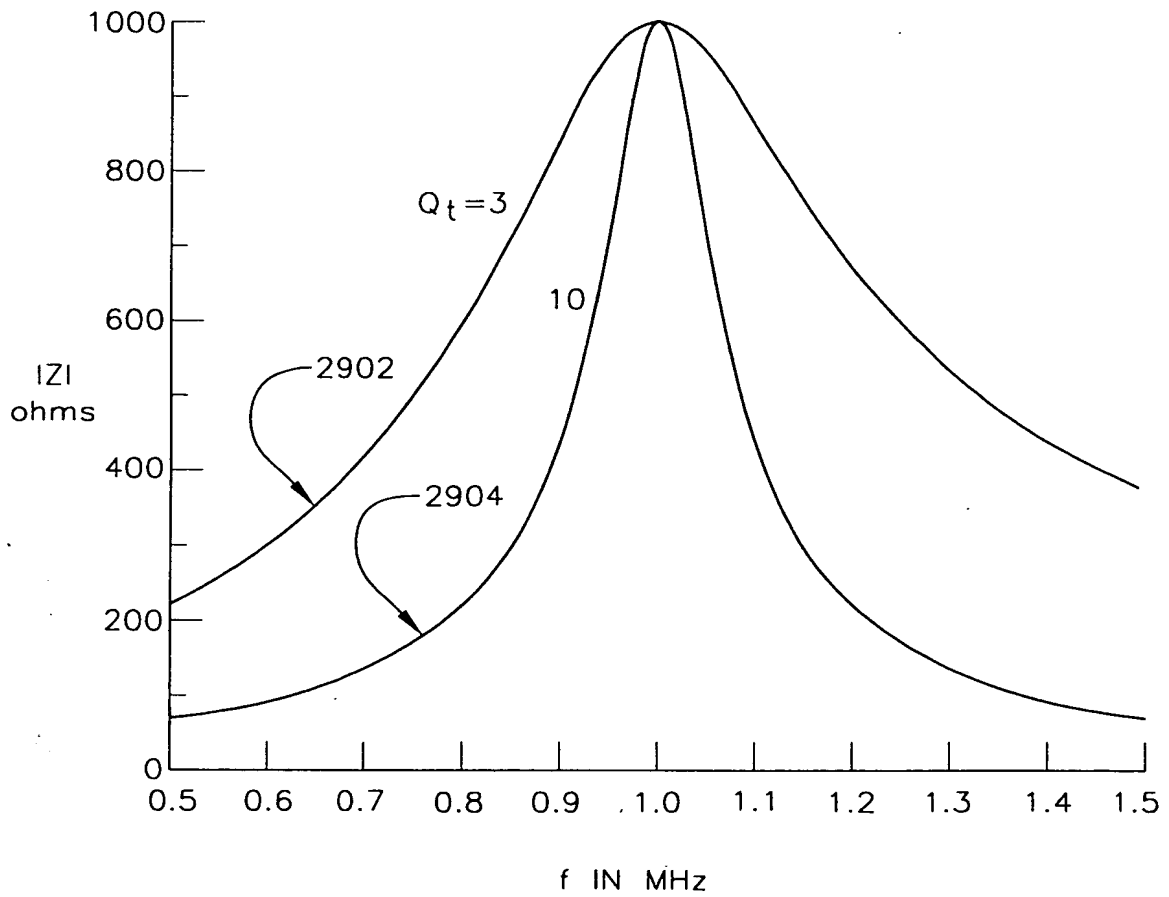




FIG. 30

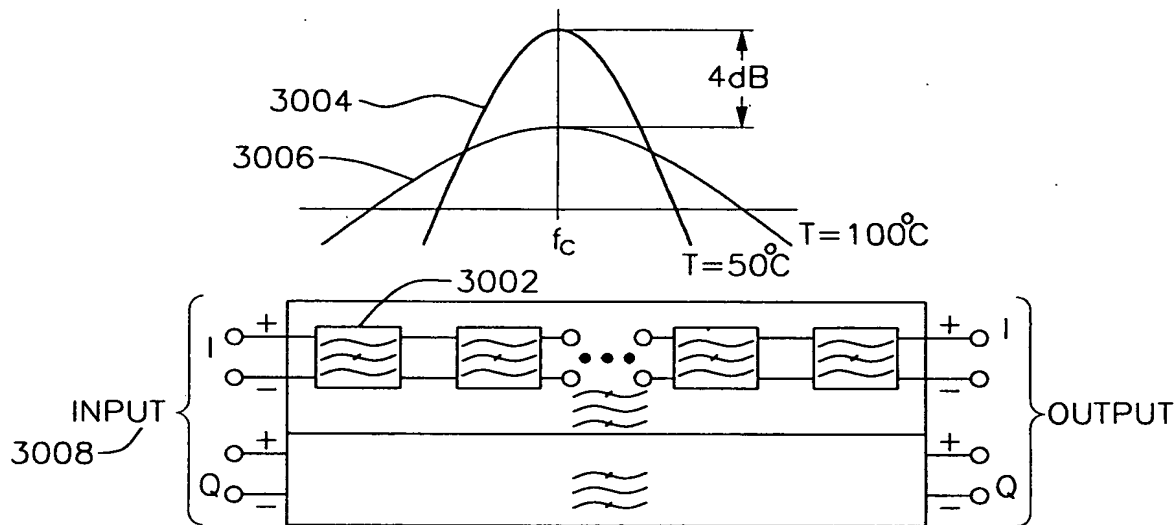
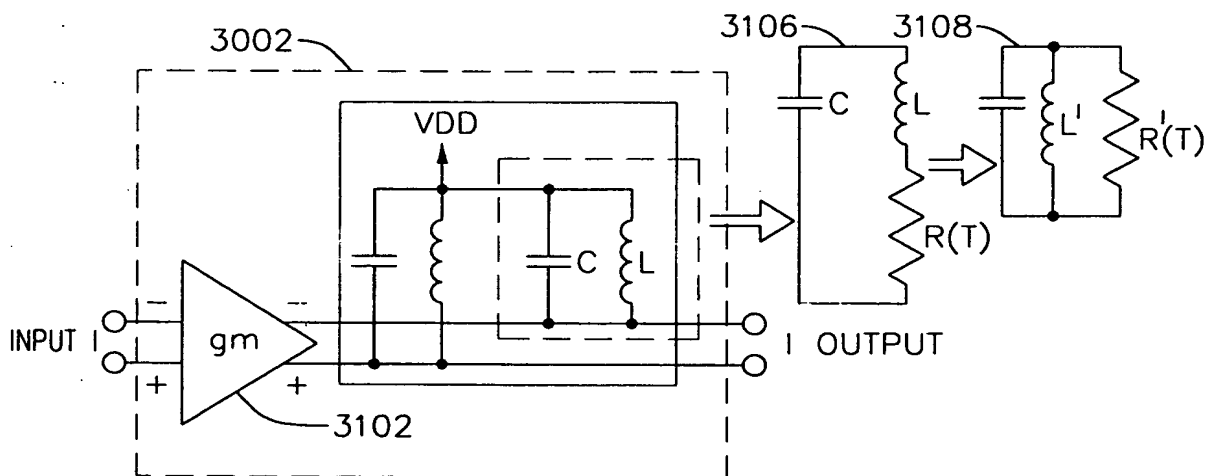


FIG. 31



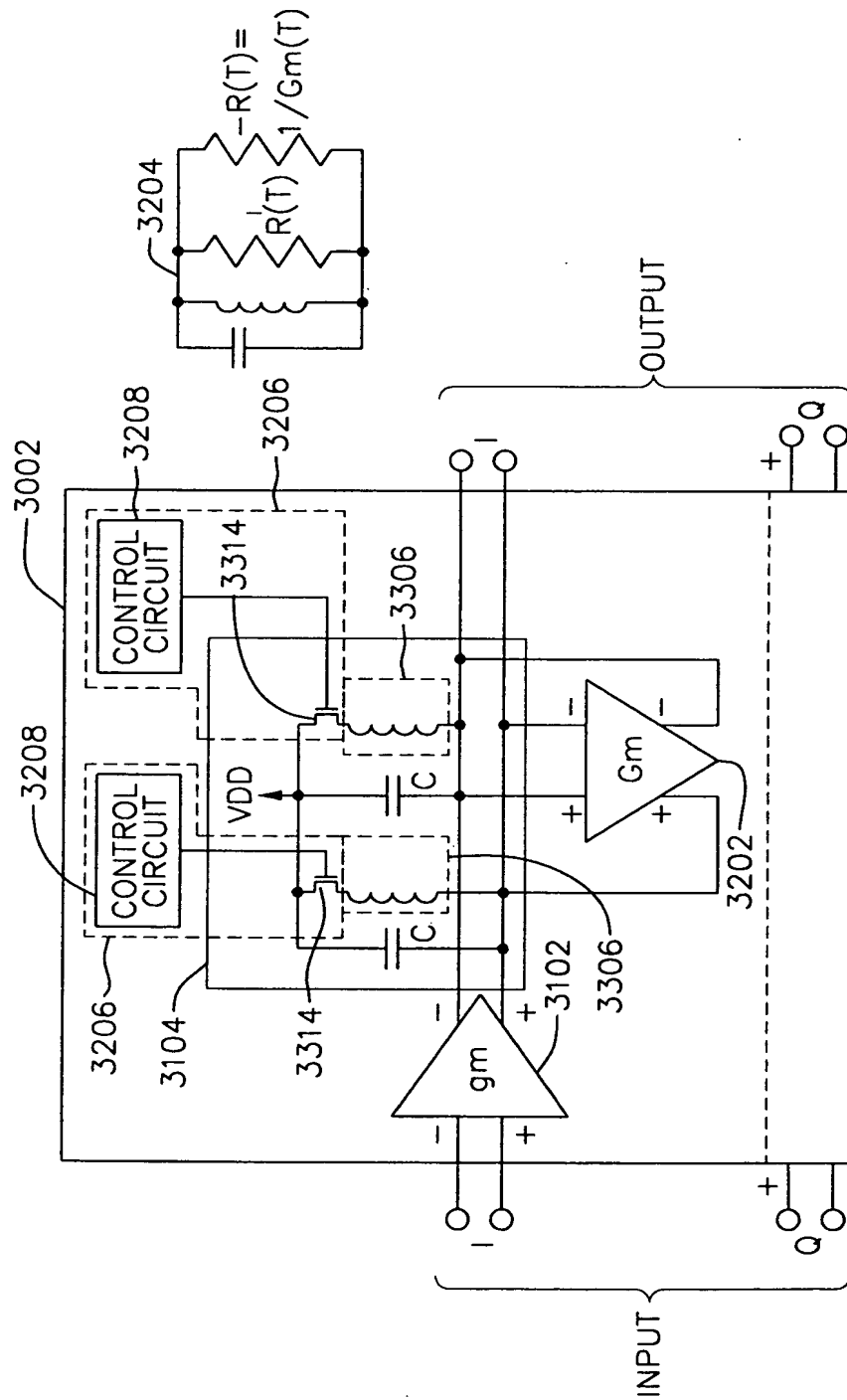
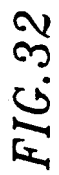




FIG. 33

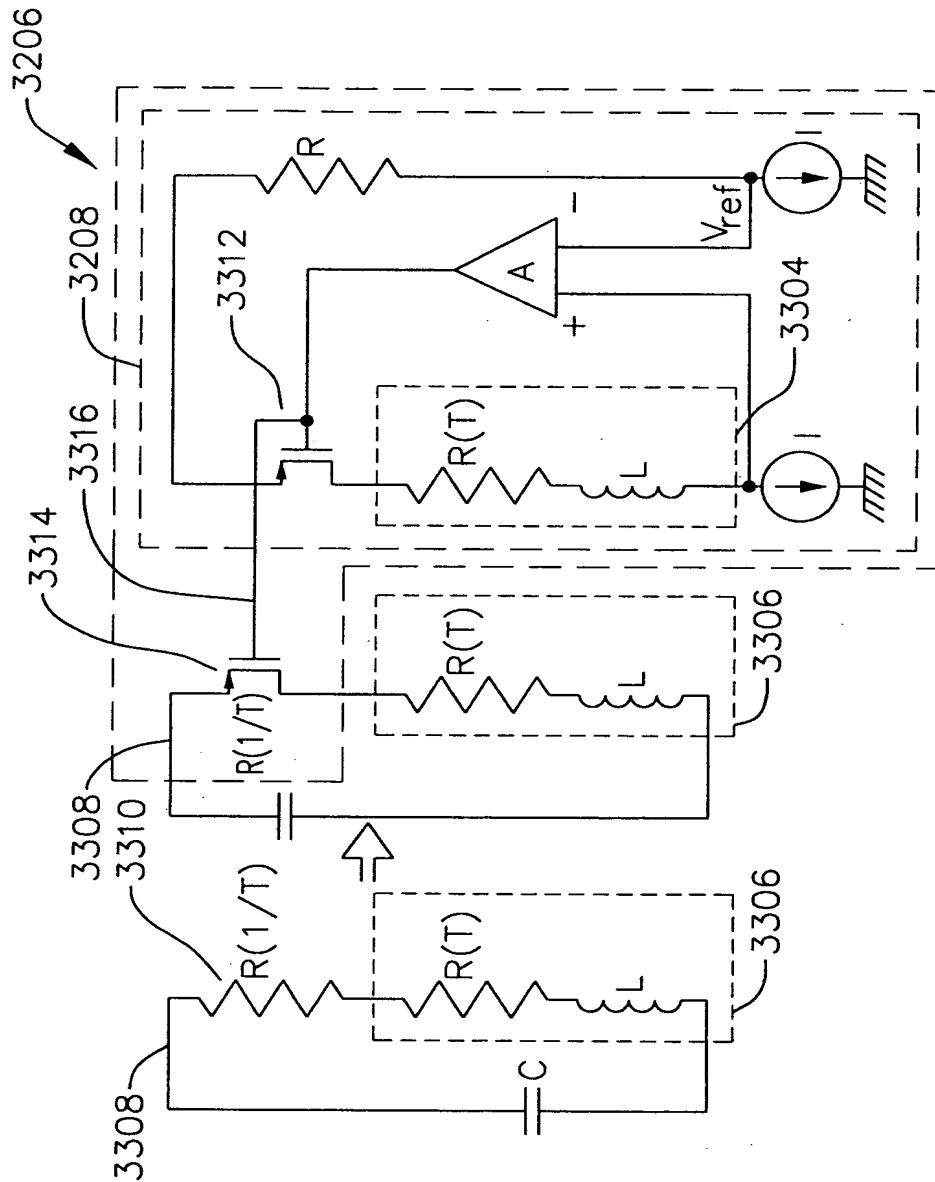




FIG.34

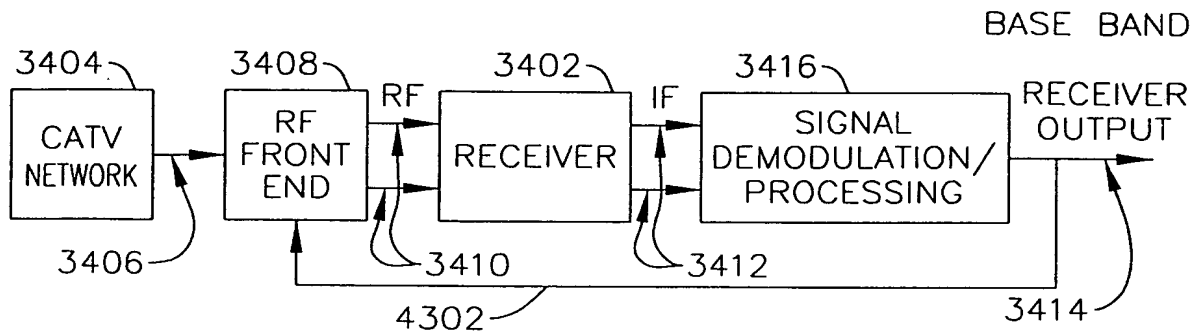


FIG.35

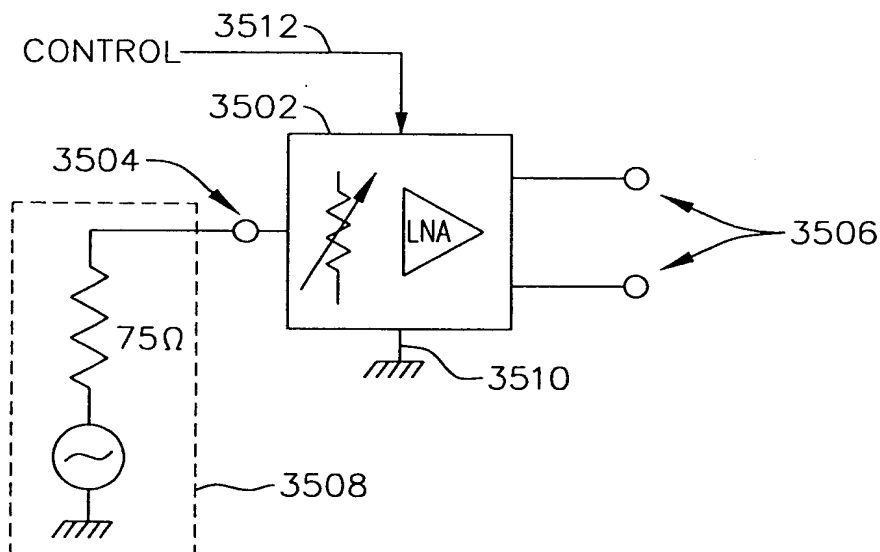




FIG. 36

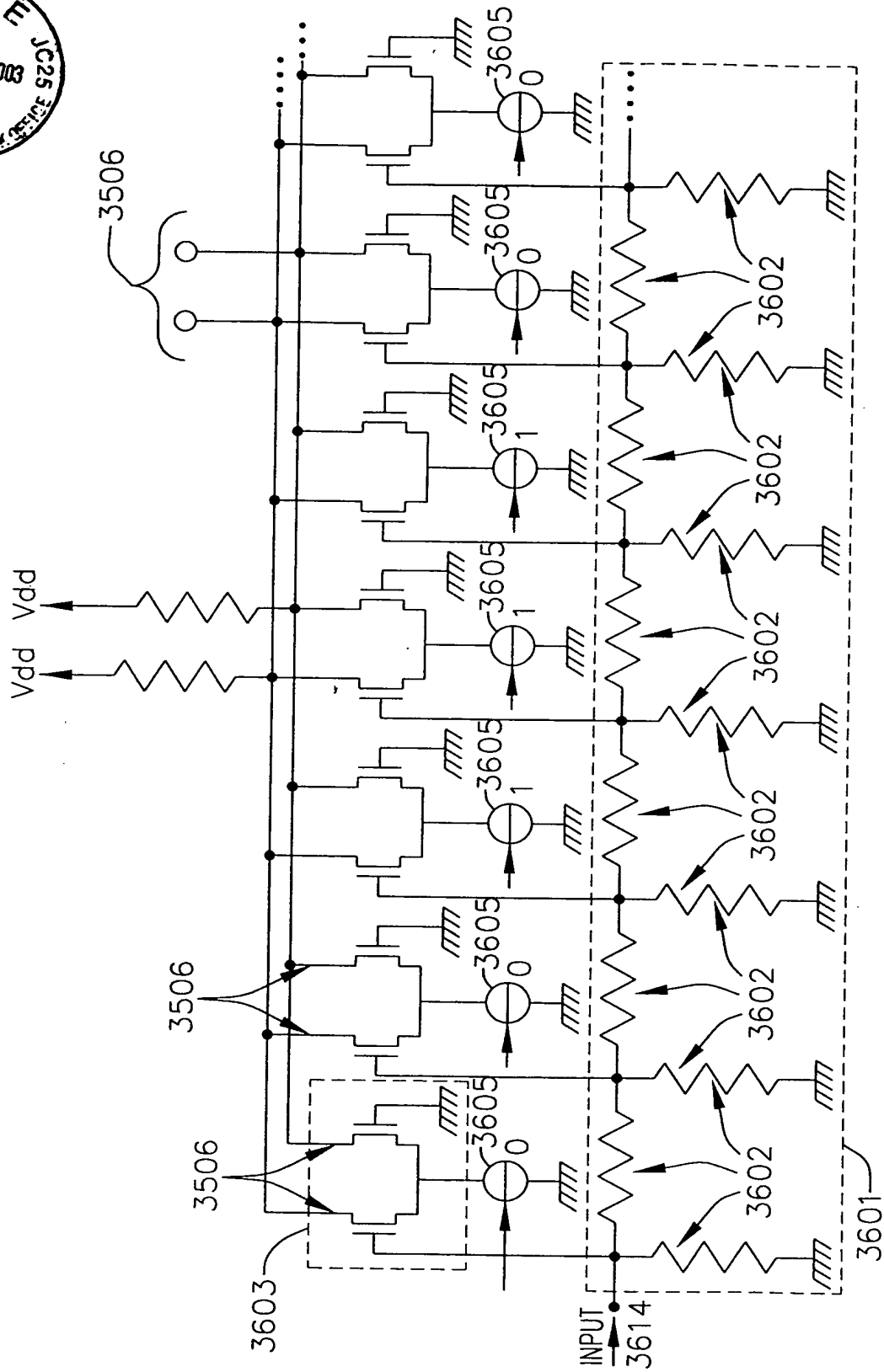
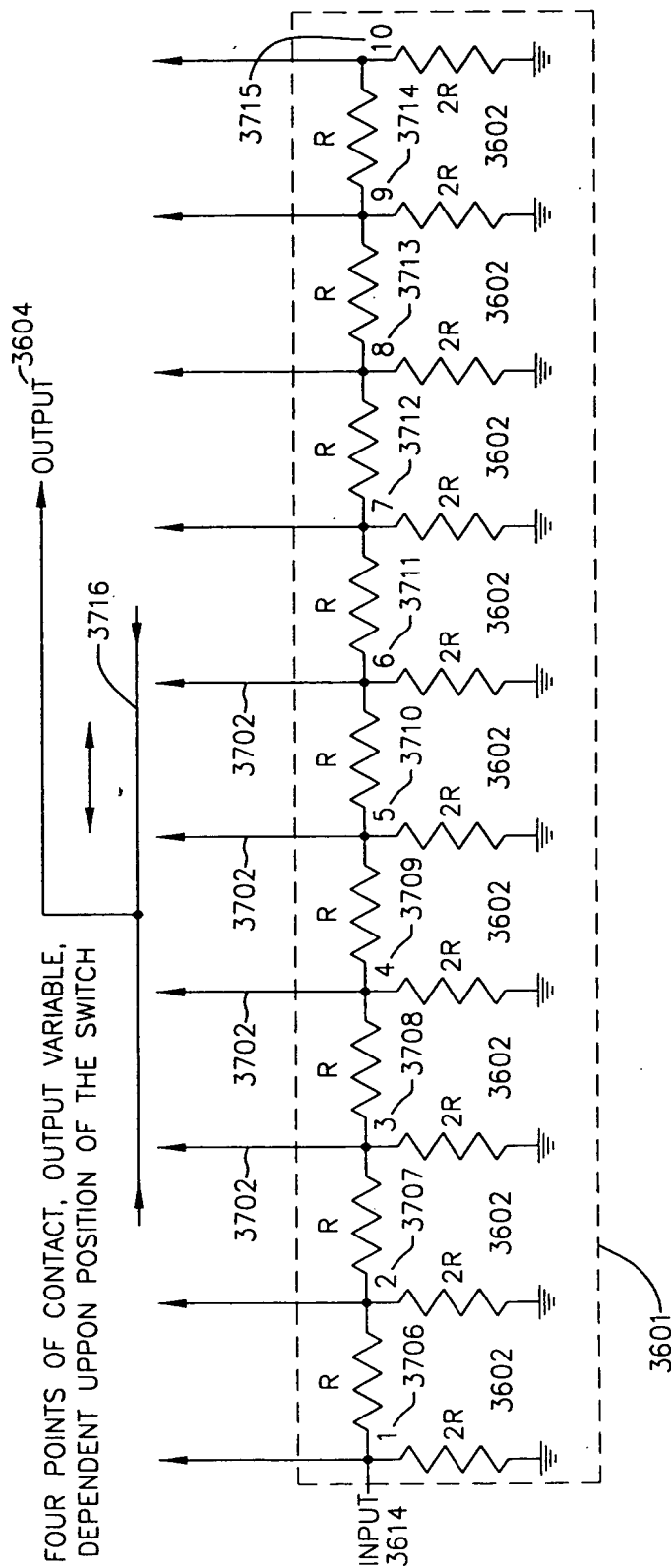




FIG. 37



A circular stamp from the Intellectual Property Office (IPO). The text "IPO" is at the top, "JUN 24 2003" is in the center, and "PATENT & TRADE MARK OFFICE" is at the bottom.

FIG. 38

PGA SETTINGS

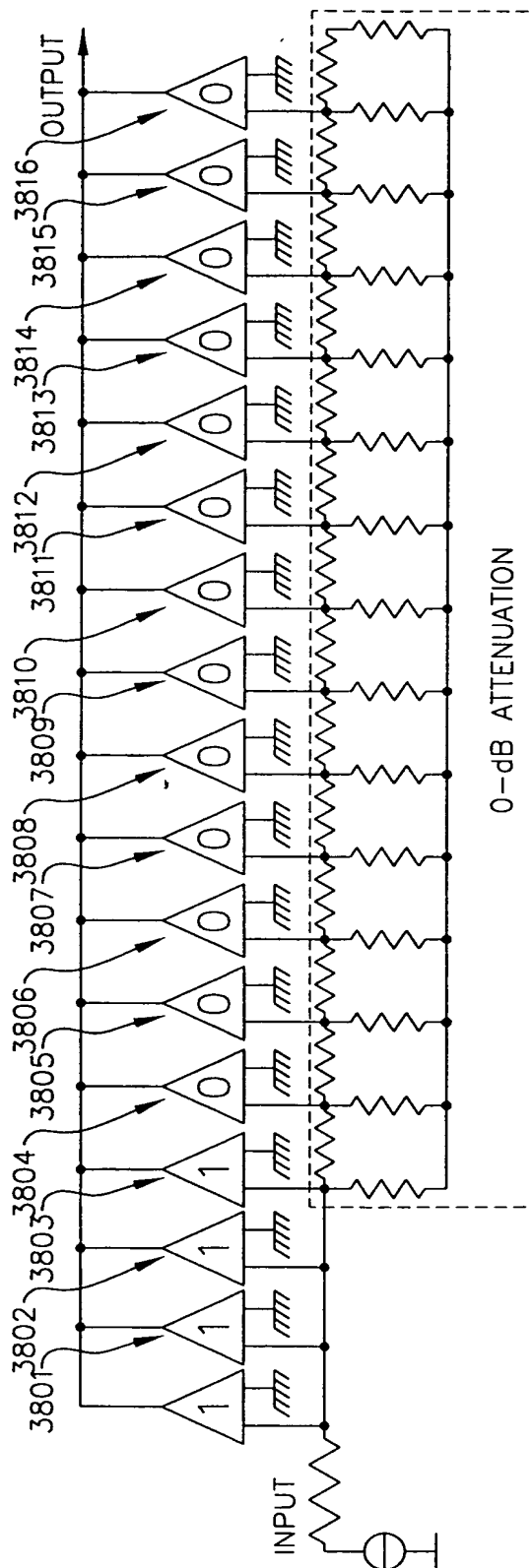




FIG. 39

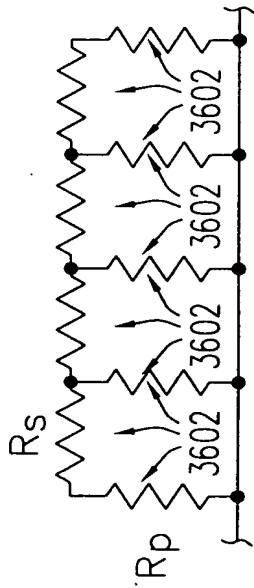


FIG. 40

PGA ARCHITECTURE

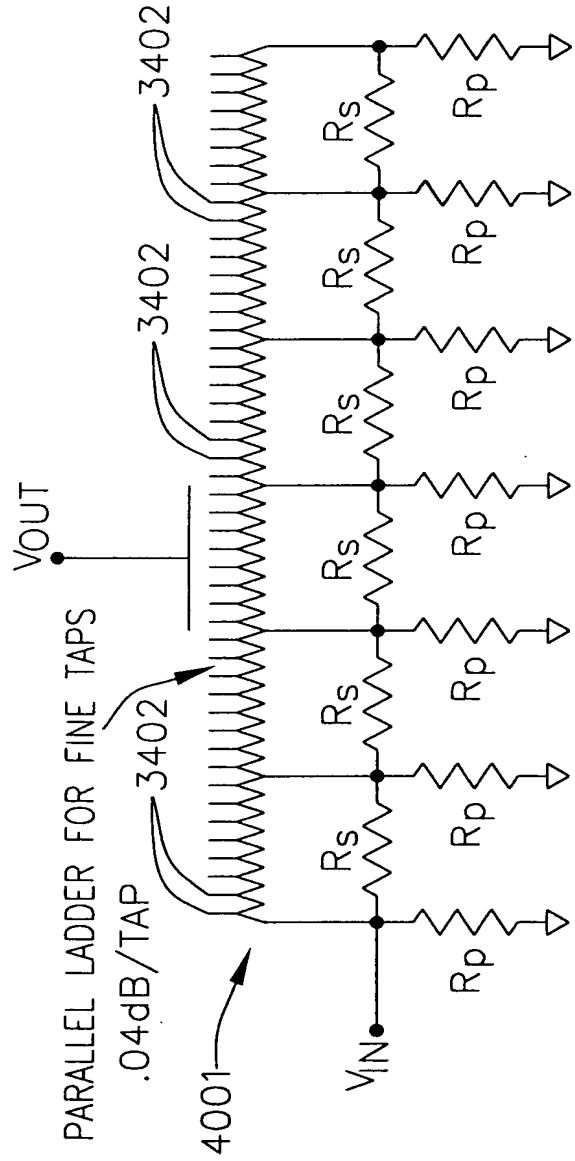




FIG. 41

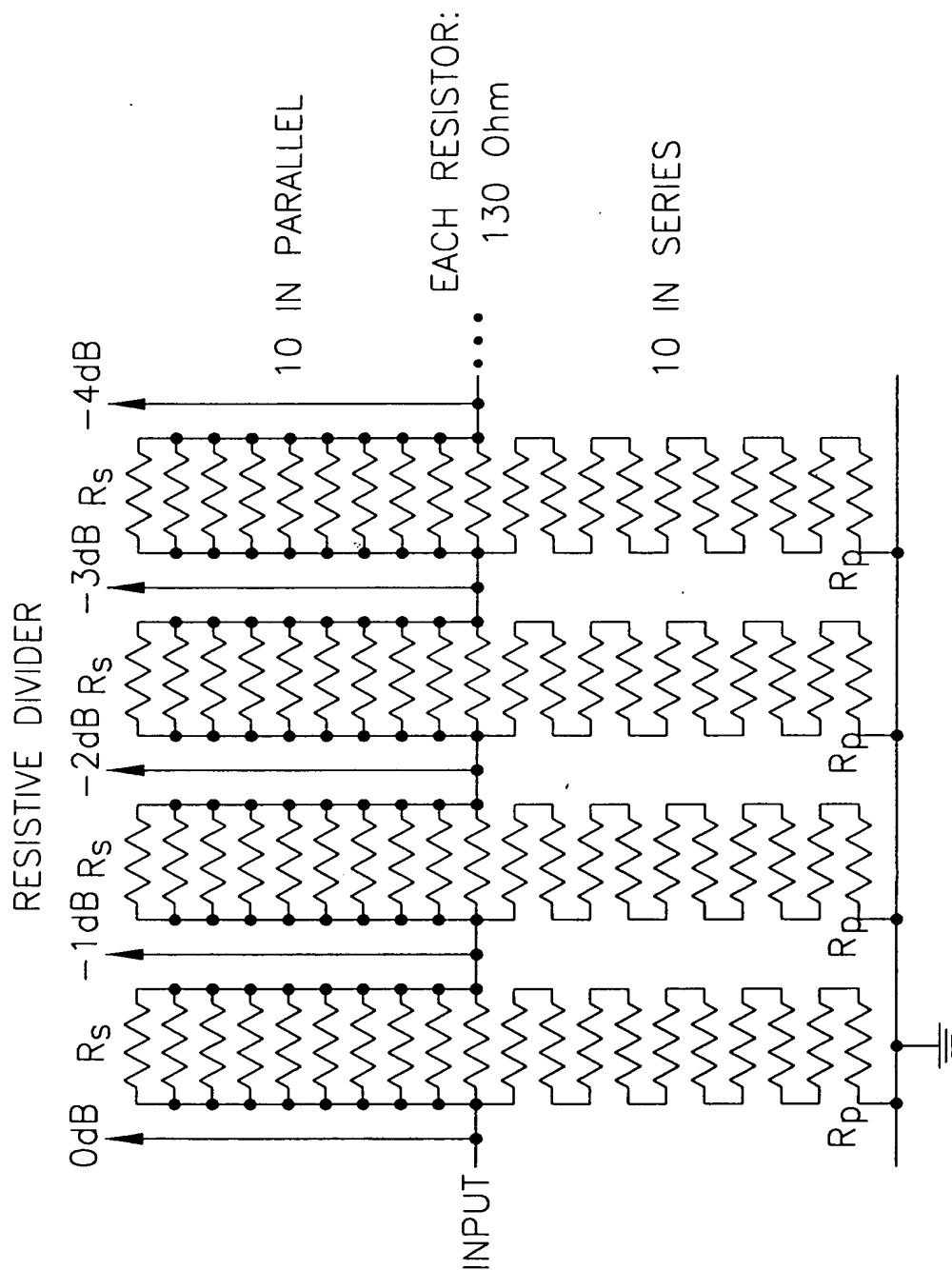




FIG. 42

NON-MONOTONICITY

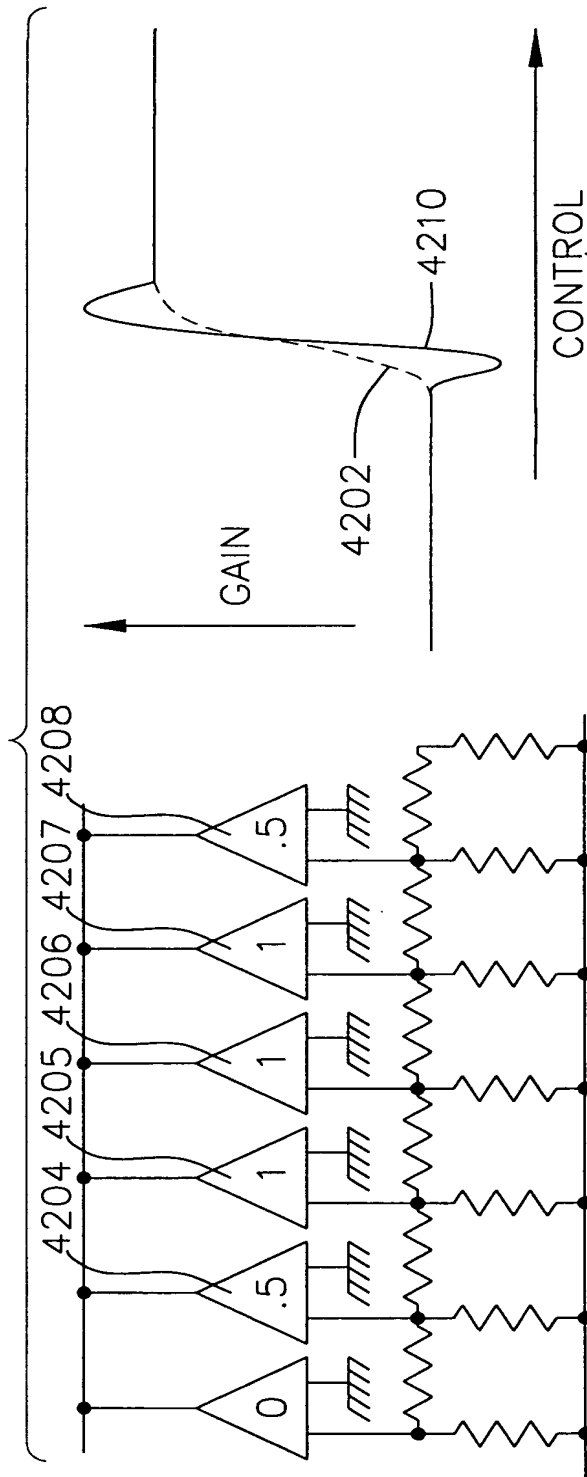
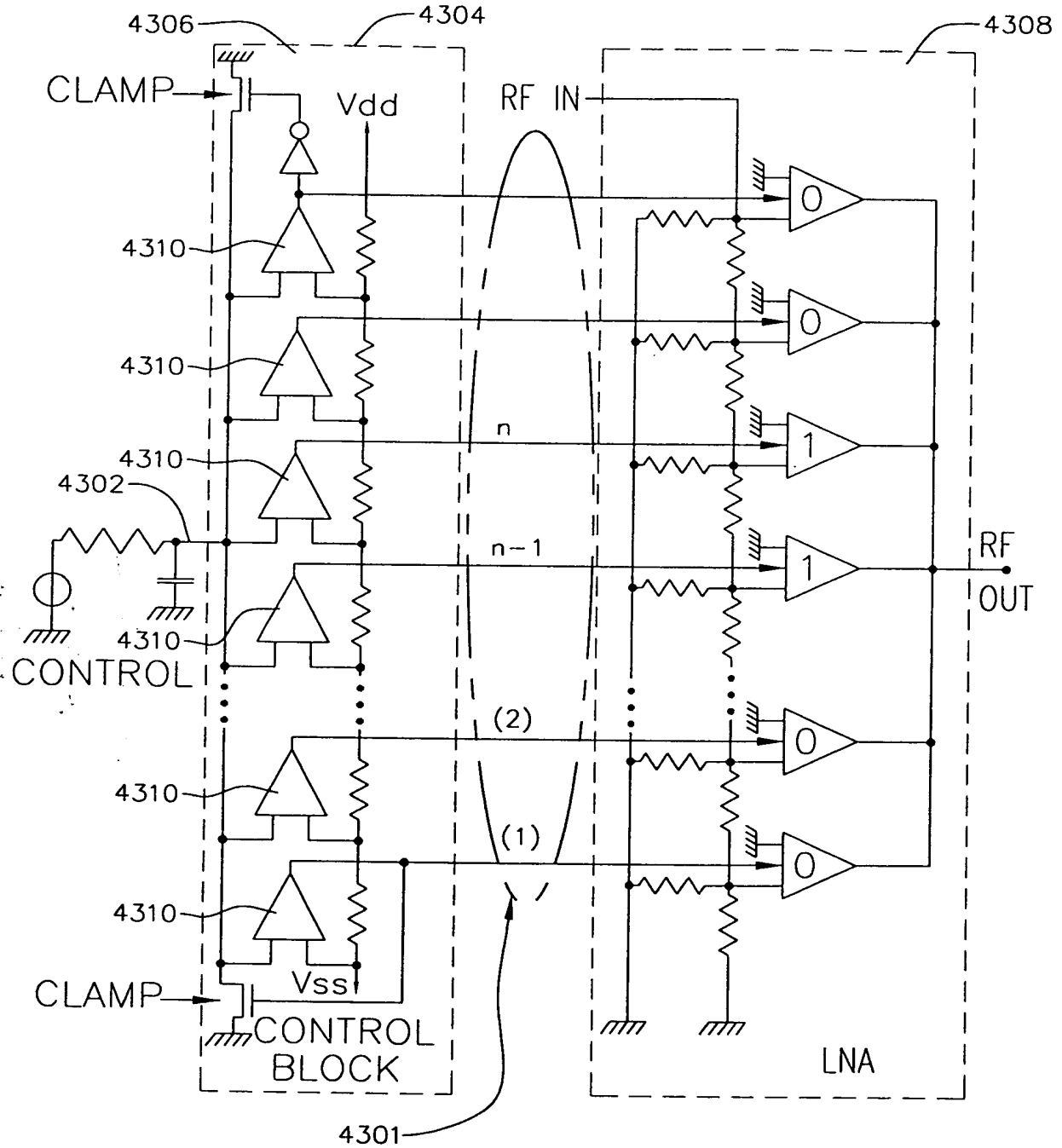


FIG. 43

CLAMPING CONTROL RANGE



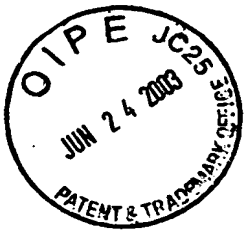
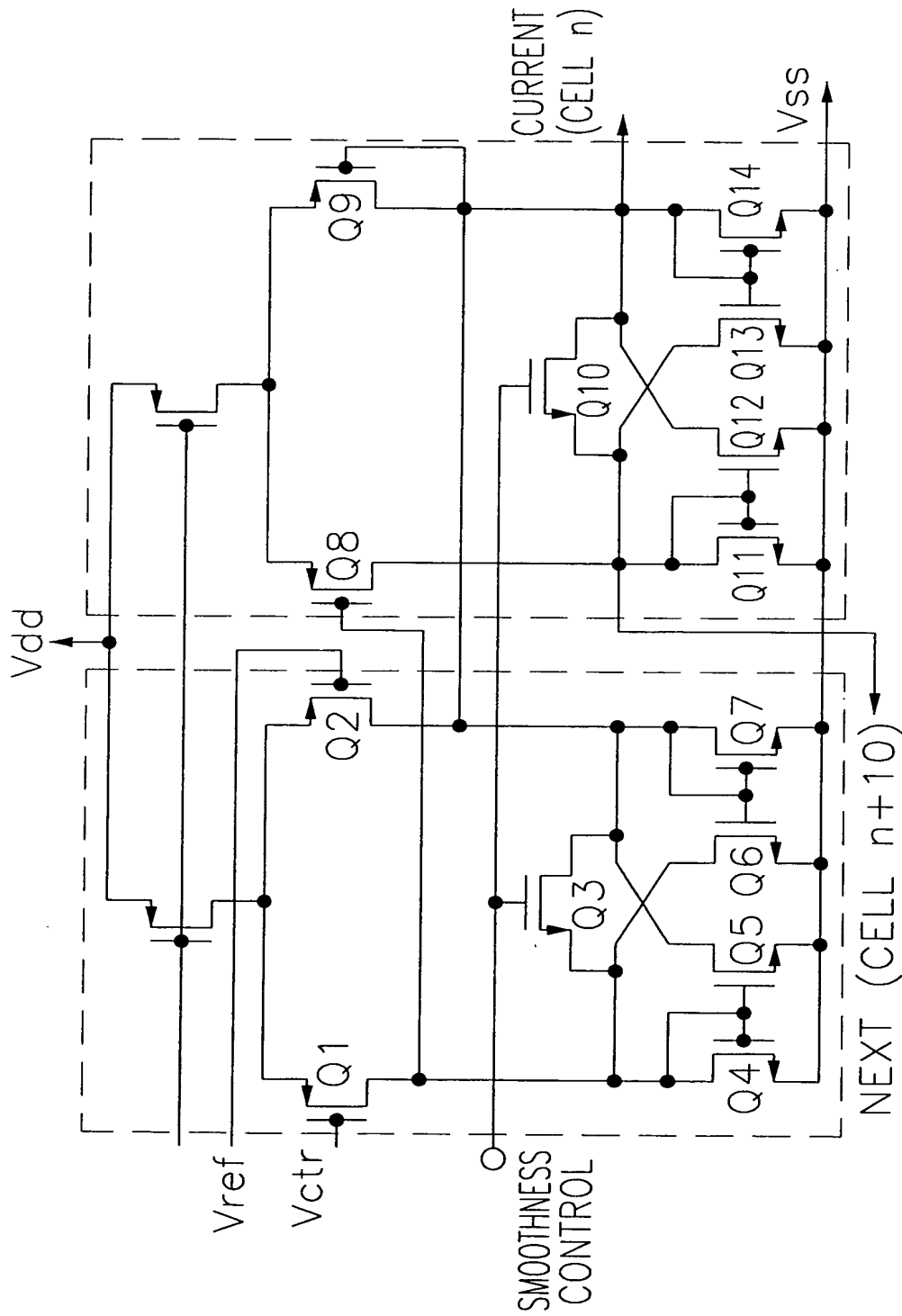


FIG. 44a
CONTROLLED GAIN COMPARATOR



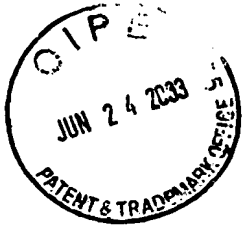


FIG. 44b

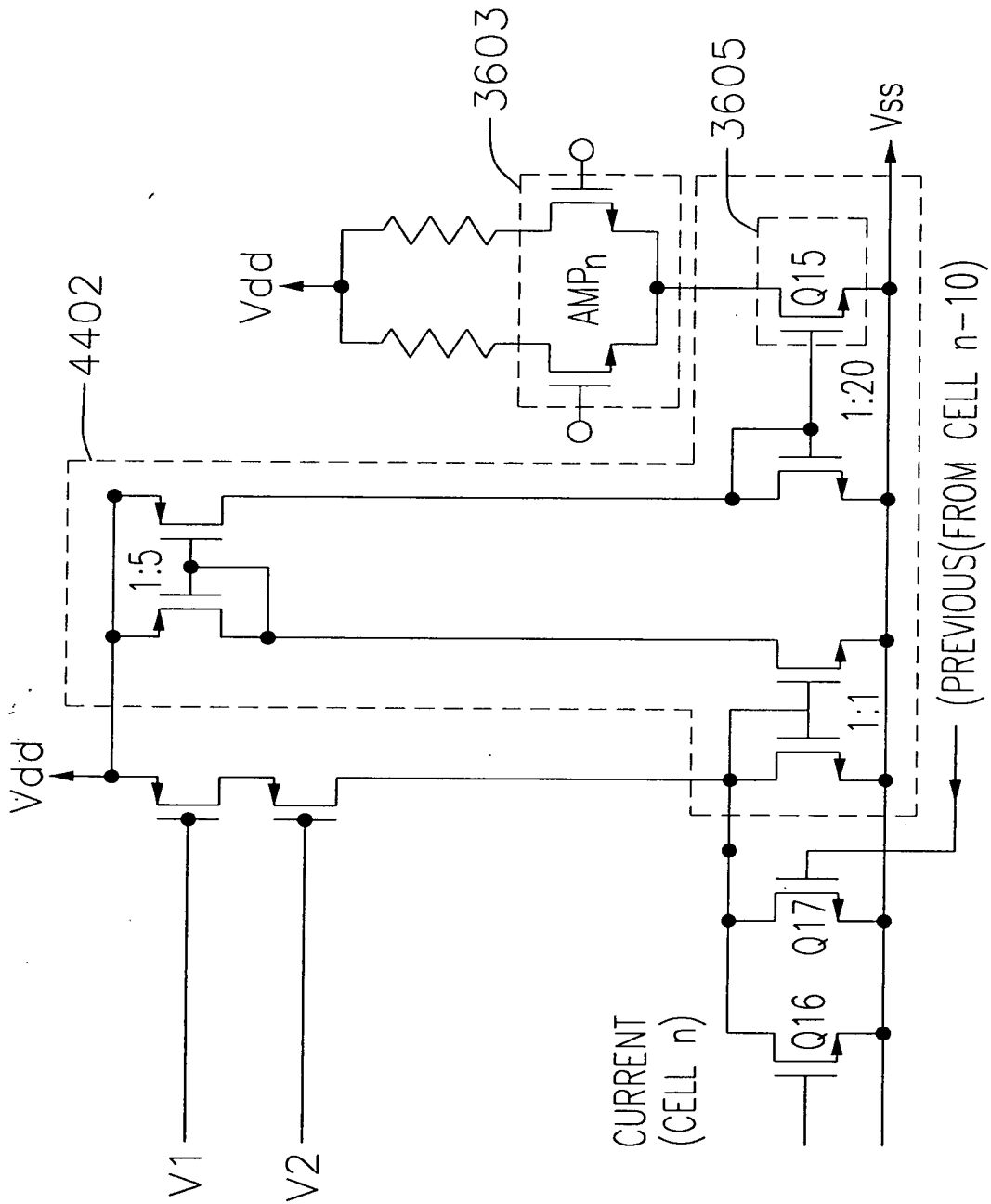
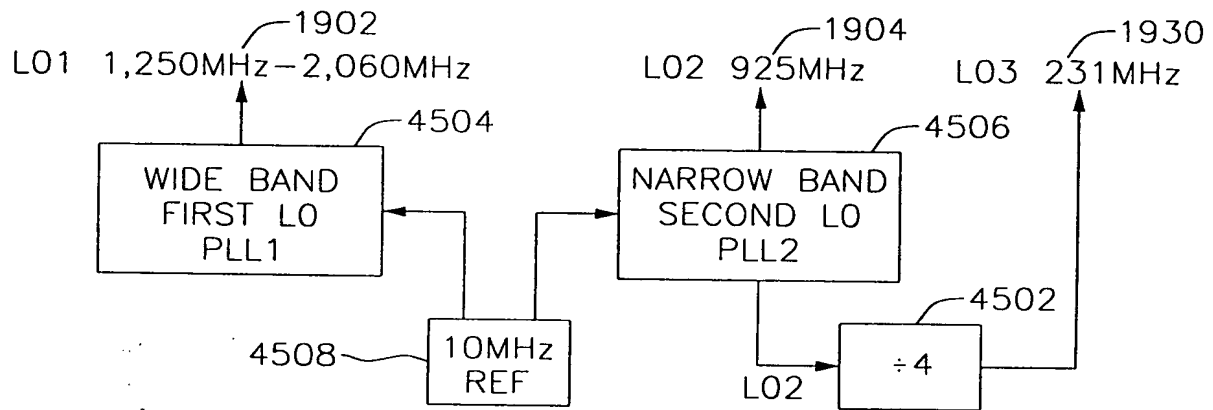




FIG. 45



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FIG. 46

The diagram illustrates a PLL system with the following components and connections:

- Reference Frequency Section:** XTAL (4606) provides a signal to a REF DIVIDER (4610). The output of the divider is split into two paths: one through a 2-bit selector (4608) to a multiplier (4612), and another through a 2-bit selector (4616) to a PUMP (4622). The output of the multiplier (4614) is the product of the reference frequency and the tuning register output.
- VCO Section:** The product signal (4614) is fed into a VCO (4618). The VCO output is split into two paths: one through a 2-bit selector (4620) to the PUMP (4622), and another through a 2-bit selector (4624) to the 6-BIT BI-DIRECTIONAL TUNING REGISTER (4628).
- Control Logic Section:**
 - A COUNTER (4632) receives a SLOWCLK signal and outputs a 6-bit signal (4634) to the MUX (4640).
 - The MUX (4640) selects between the product signal (4614) and the VCO output (4624) based on the 6-bit signal (4634).
 - The output of the MUX is fed into a DETECTOR (4648), which outputs an INLOCK signal.
 - The DETECTOR output is also fed into a 6-bit signal (4644) that is fed back to the 6-BIT BI-DIRECTIONAL TUNING REGISTER (4628).
 - The 6-BIT BI-DIRECTIONAL TUNING REGISTER (4628) has a 0/1 input and a 6-bit output (4630) that is fed back to the MUX (4640).
 - The 6-BIT BI-DIRECTIONAL TUNING REGISTER (4628) also has a 6-bit output (4636) that is fed back to the COUNTER (4632).
 - The 6-BIT BI-DIRECTIONAL TUNING REGISTER (4628) has a 6-bit output (4638) that is fed back to the VCO (4618).
- Other Components:** A MUX (4640) selects between the product signal (4614) and the VCO output (4624) based on the 6-bit signal (4634). A DETECTOR (4648) outputs an INLOCK signal. A 6-BIT BI-DIRECTIONAL TUNING REGISTER (4628) has a 0/1 input and a 6-bit output (4630) that is fed back to the MUX (4640).

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FIG. 47

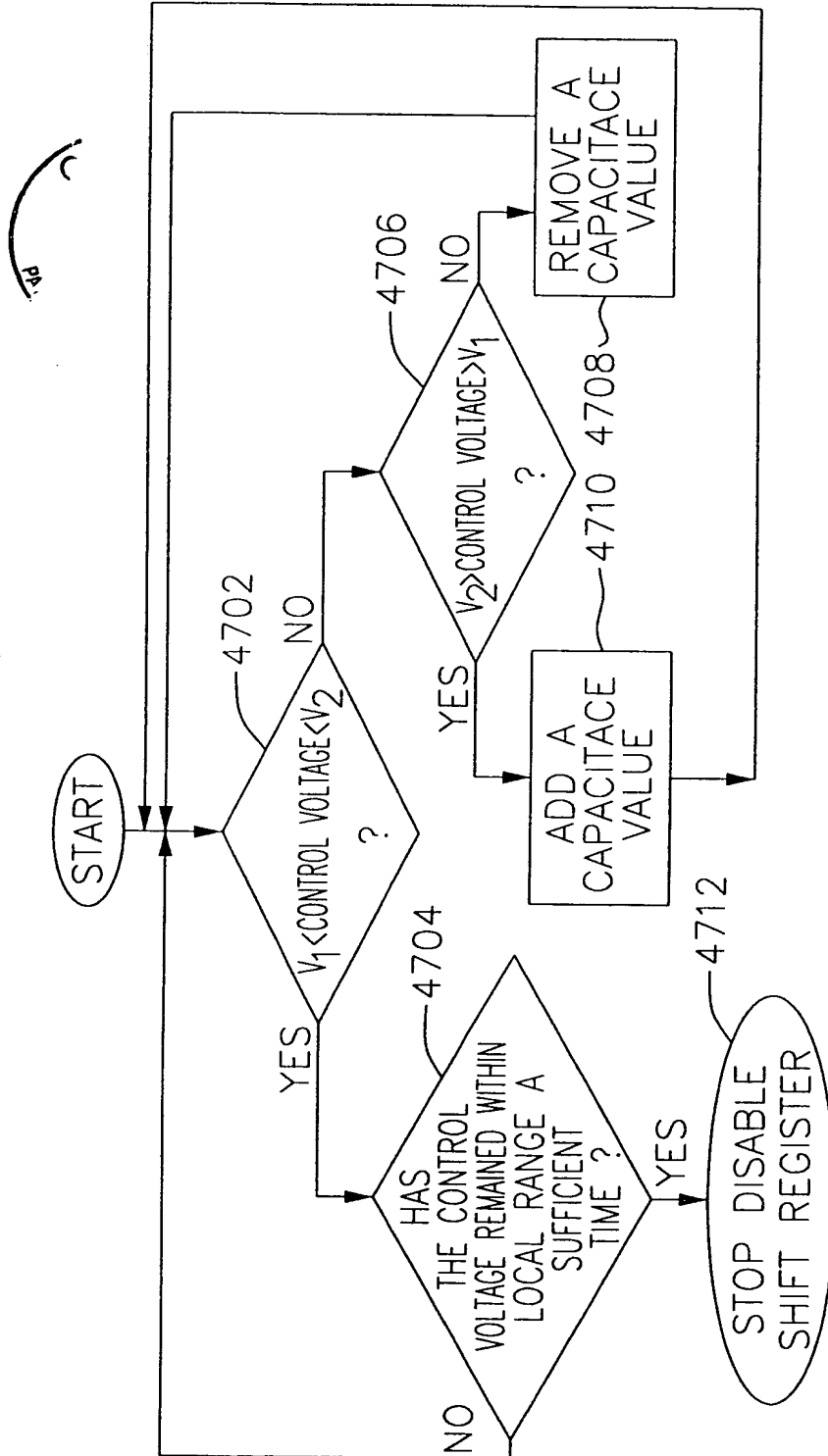




FIG. 48

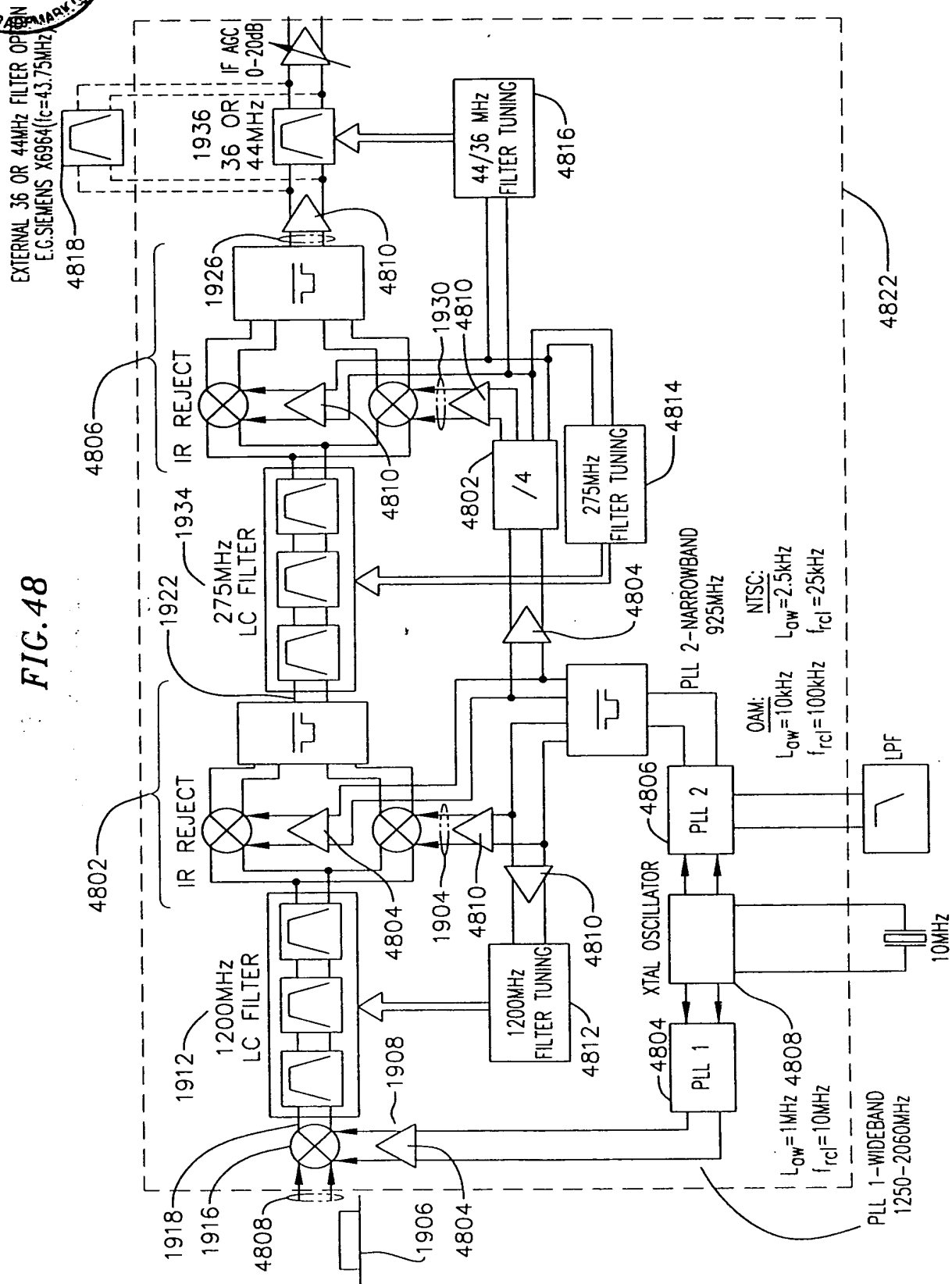




FIG. 49

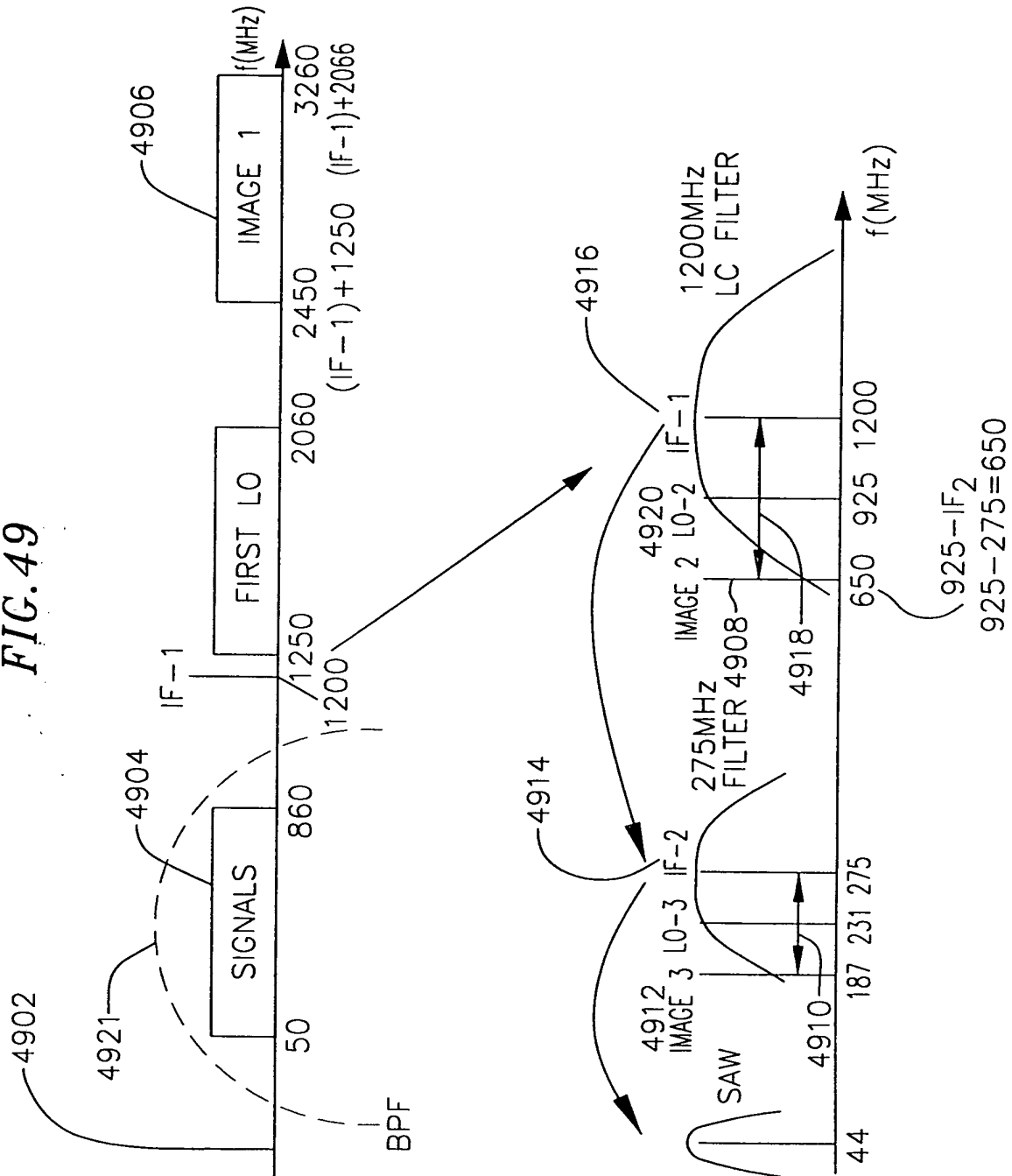
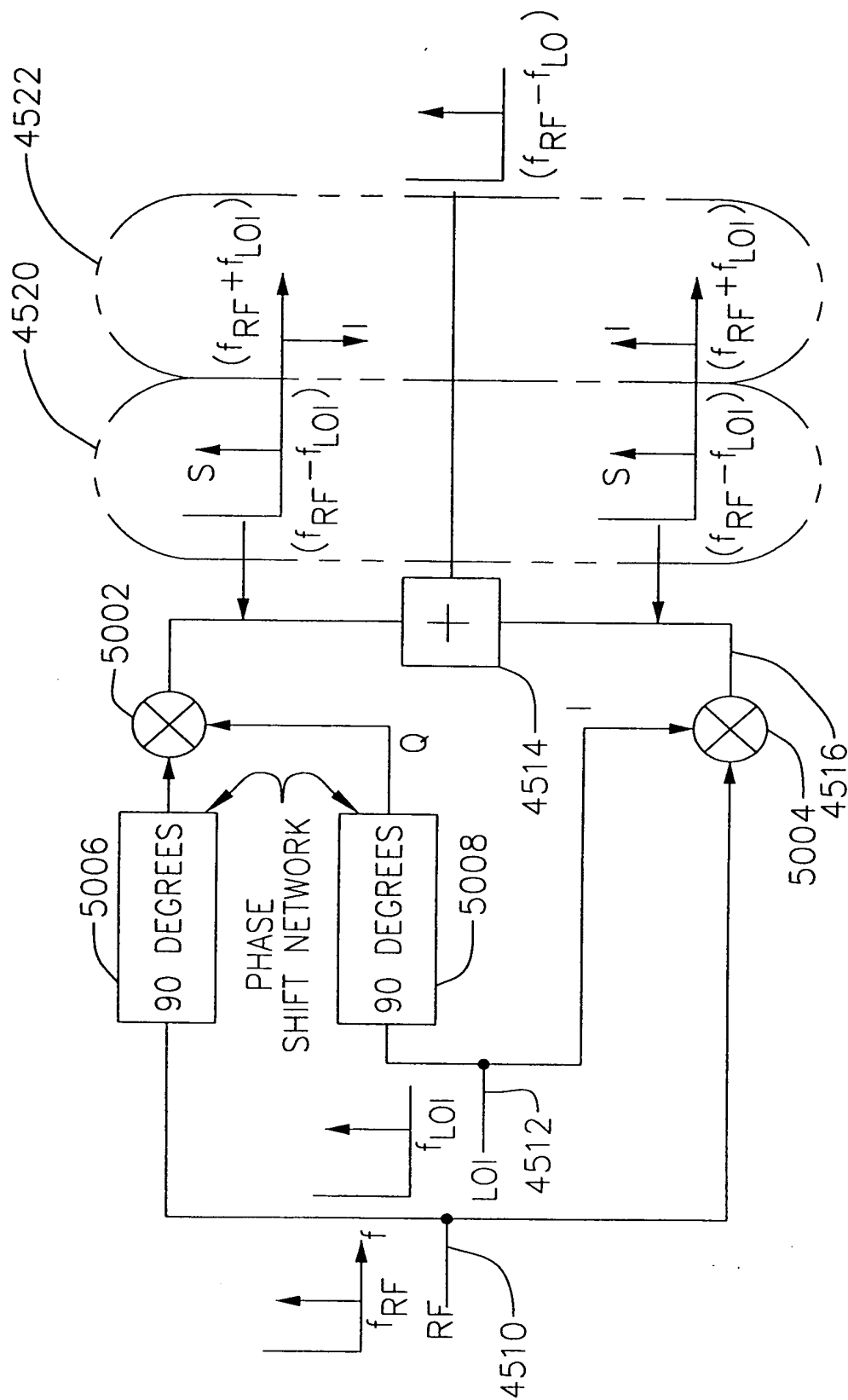




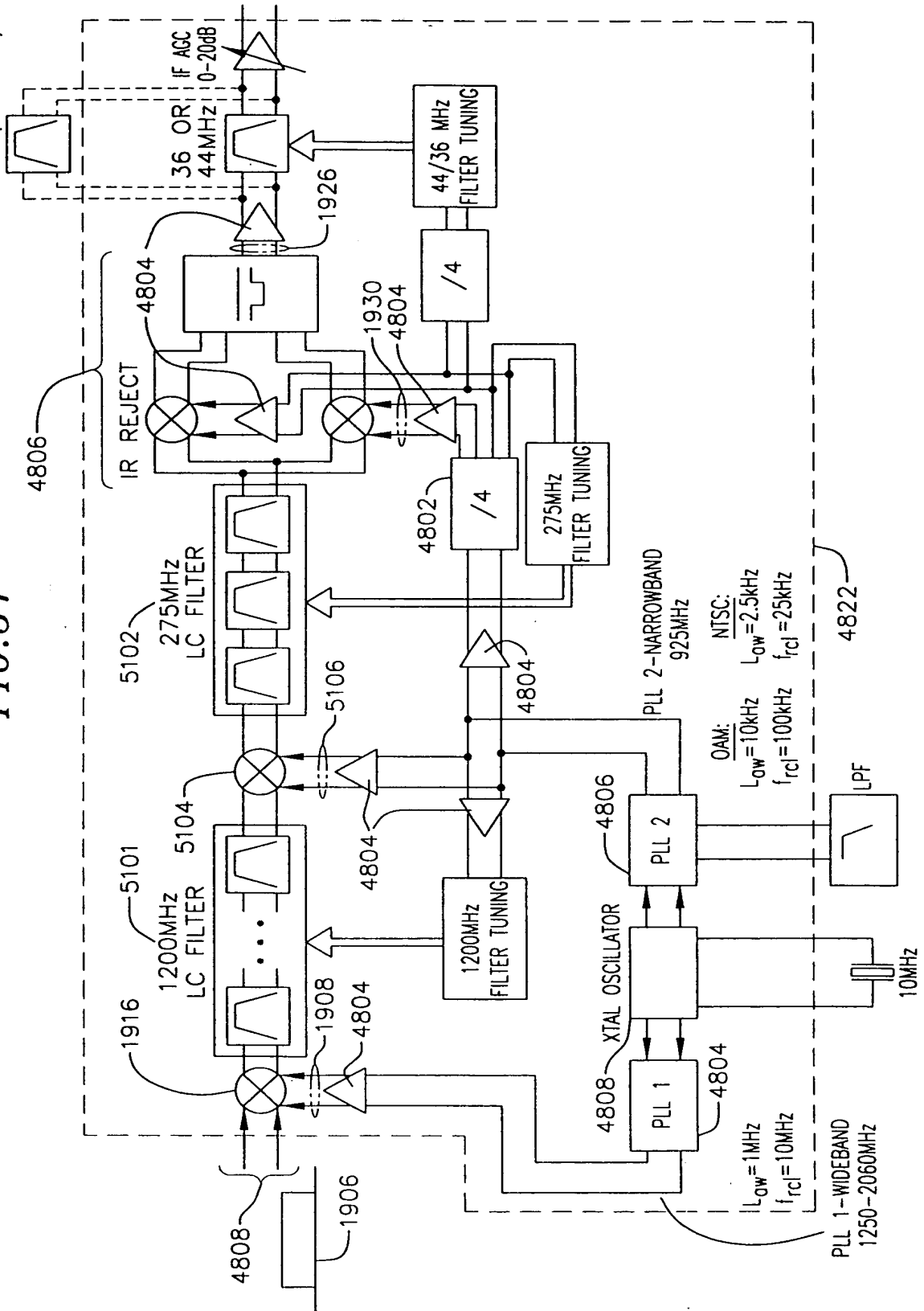
FIG. 50





EXTERNAL 36 OR 44MHz FILTER OPTION
 E.G. SIEMENS X6964 ($f_c = 43.75\text{MHz}$)

FIG. 51



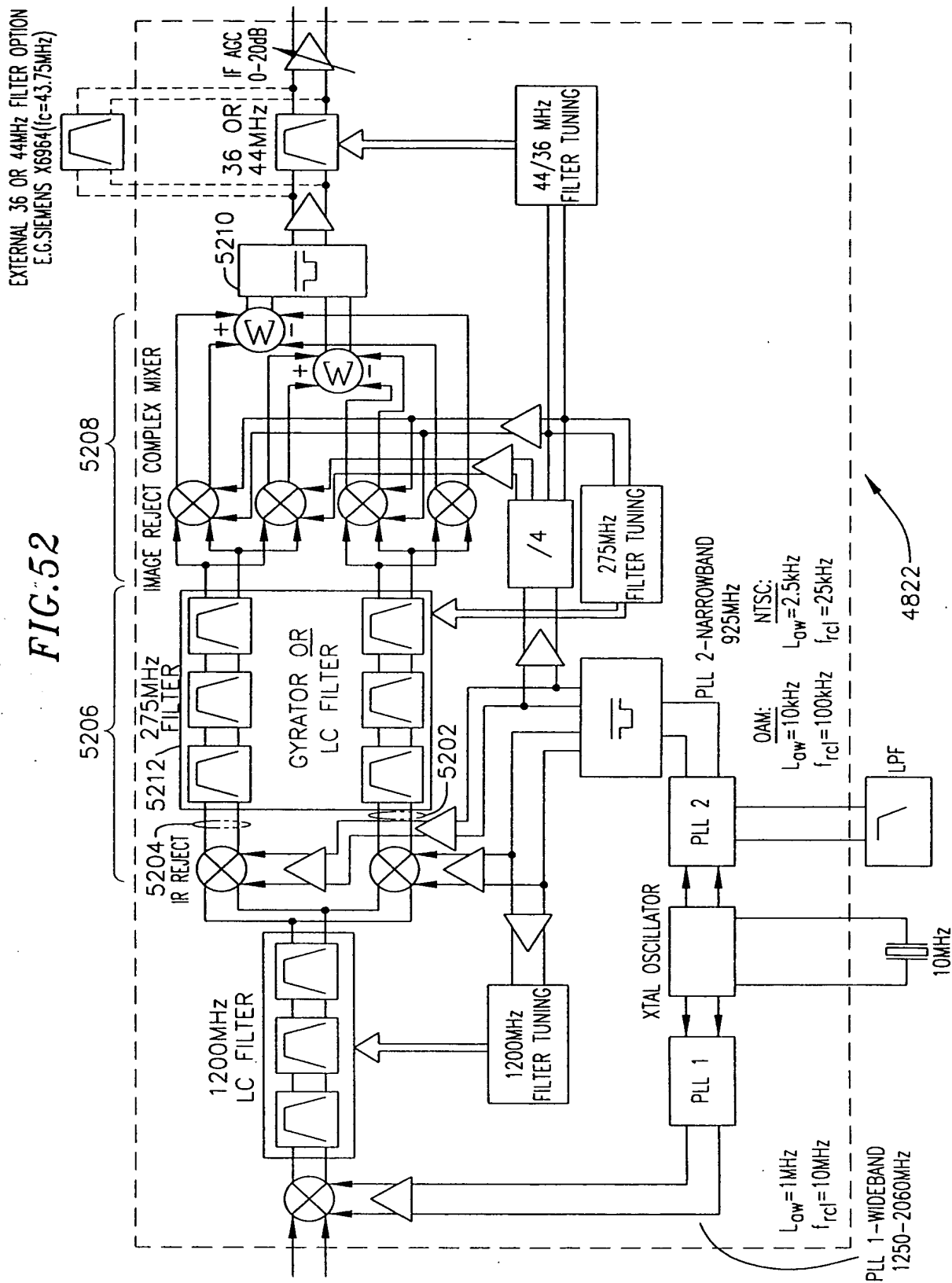


FIG. 53

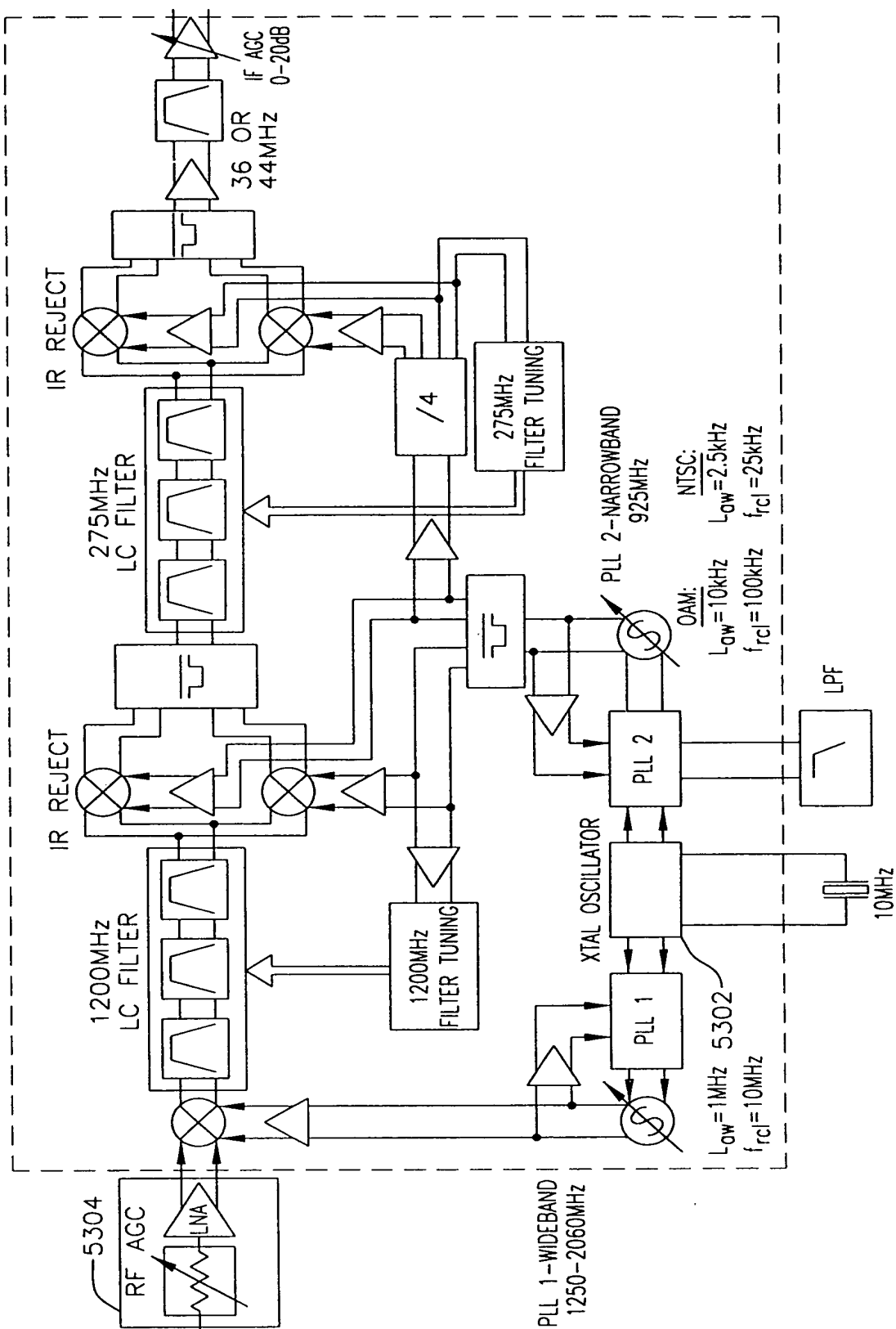




FIG. 54

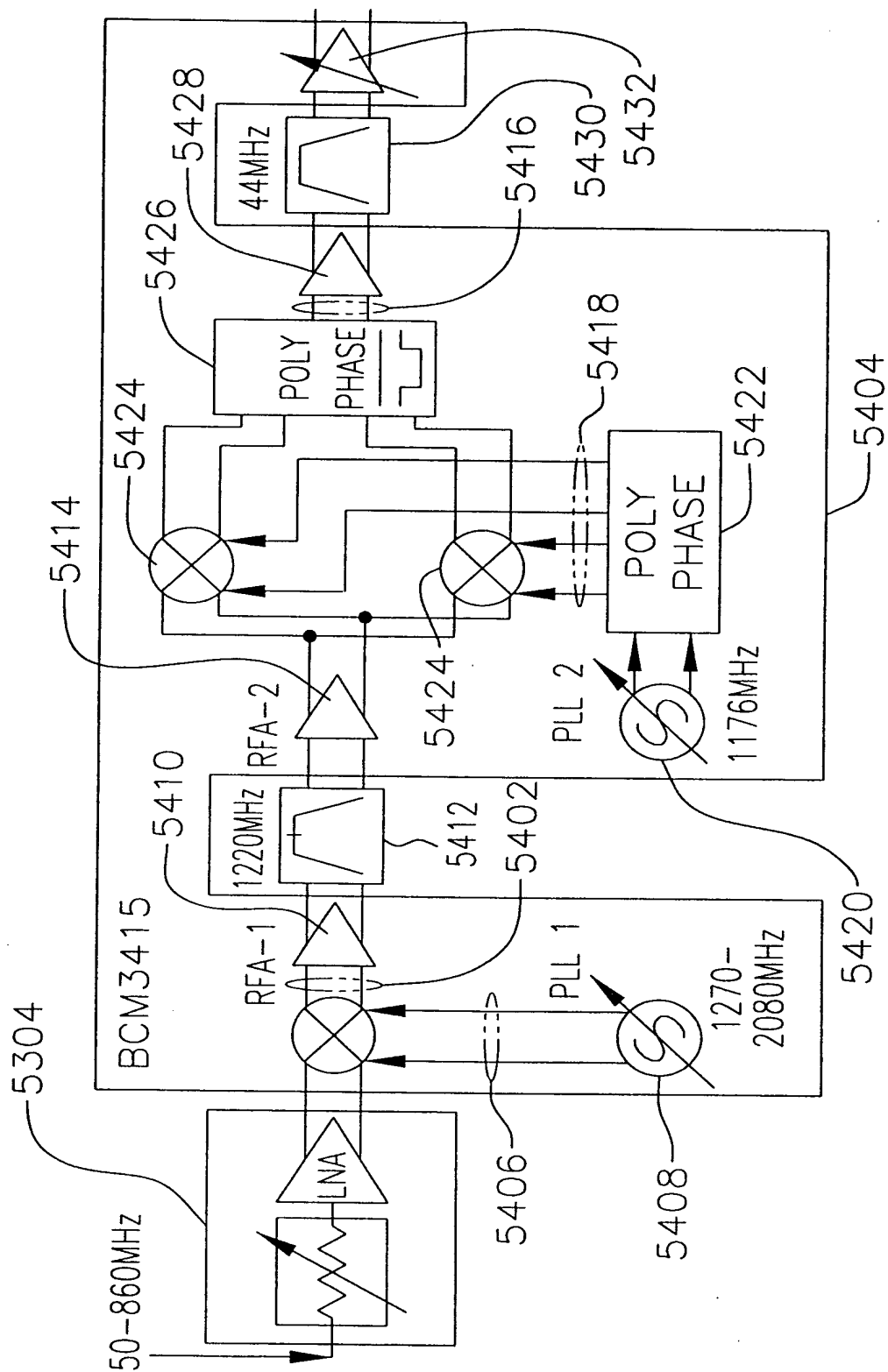
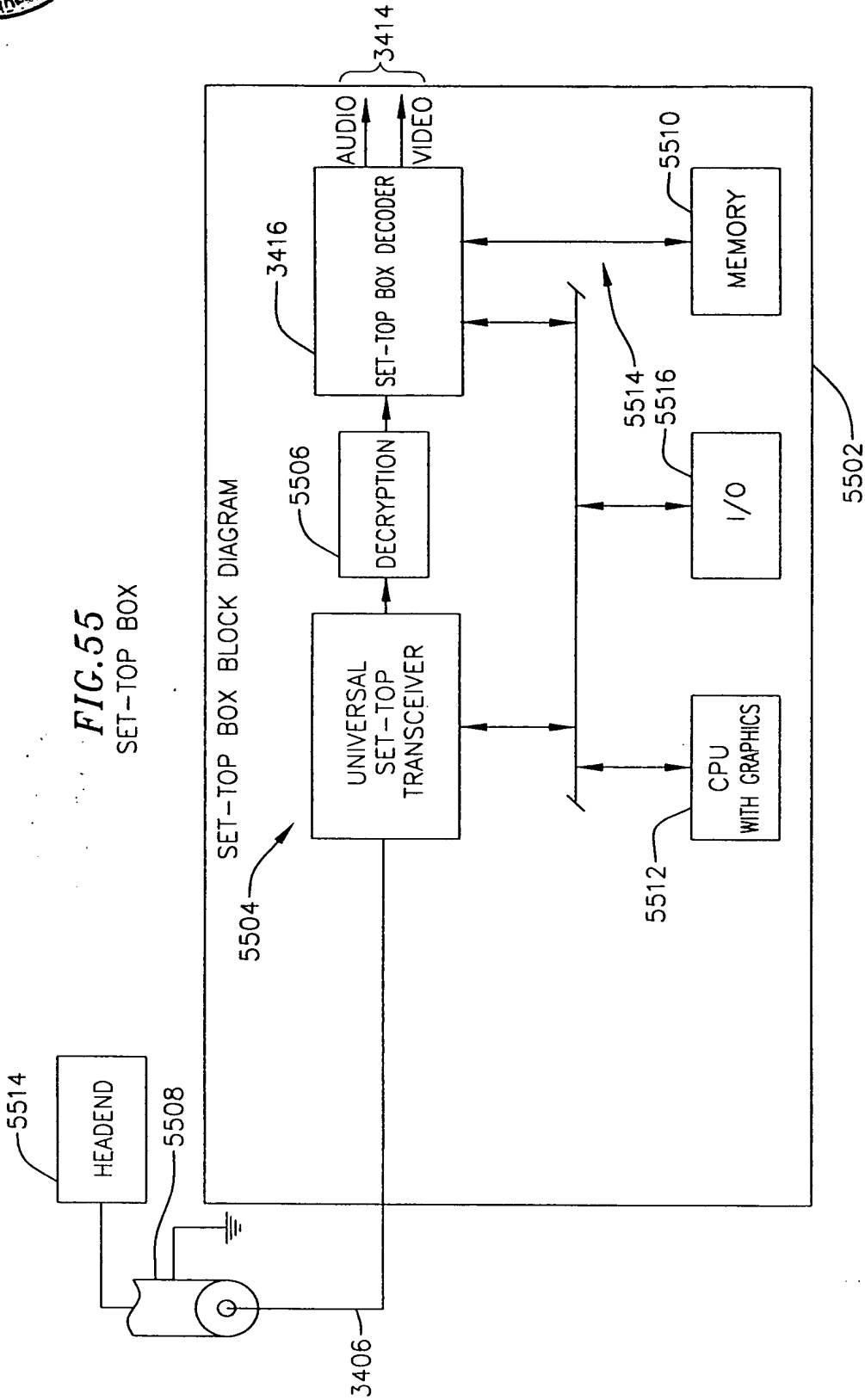




FIG. 55
 SET-TOP BOX



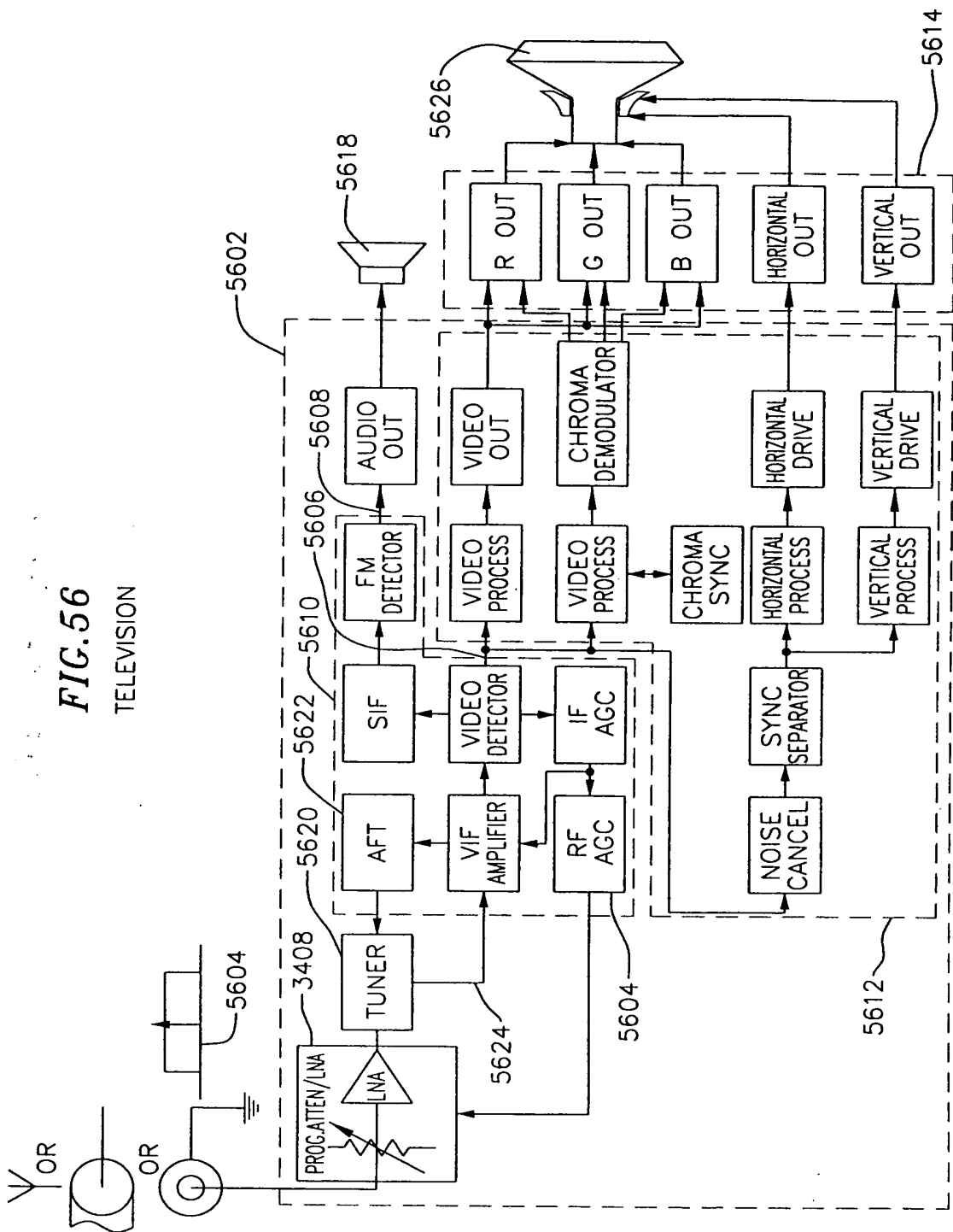




FIG. 57
 VCR BLOCK DIAGRAM

